

# **GMB-C2165-LLVA**

## **Industrial Motherboard ATX Board**

### **User's Manual** Version 1.0



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## How to Use This Manual

The manual describes how to configure your GMB-C2165-LLVA system board to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

**Chapter 1: System Overview.** Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

**Chapter 2: Hardware Configuration.** Show the definitions and locations of Jumpers and Connectors that you can easily configure your system.

**Chapter 3: System Installation.** Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

**Chapter 4: BIOS Setup Information.** Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

**Chapter 5: Troubleshooting.** Provide various of useful tips to quickly get GMB-C2165-LLVA running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. The vendor may make supplement or change in the products described in this document at any time

# **1. System Overview**

## **1.1. Introduction**

Powell Inc., a world-leading innovator in the Industrial PC (IPC) market and a member of the Intel® Communications Alliance, has launched its new GMB-C2165-LLVA in response to market demand for a simplified embedded system board (ESB) that combines a smaller footprint, lower power consumption, robust computing power and with longevity support.

Against the pre-generation chipset GMB-C2165-LLVA based on C216 chipset, C216 offers Core i3/Xeon processors, VGA, DVI-D, Display port, USB 3.0 and SATA III support which USB 3.0 is first integrated.

GMB-C2165-LLVA based on the latest 3rd Gen Intel® Xeon Processor which offers 22nm Hi-K process technology with energy efficient architecture. GMB-C2165-LLVA adopts four channels DDR3 long DIMMs up to 32GB.

Desktop solution is still popular in the market of DVR and Factory Automation which can fulfill most of these applications; therefore, with high performance and high-end specifications, Q77 is our first generation Ivy bridge chip architecture on

## **1.2. Check List**

The GMB-C2165-LLVA package should cover the following basic items

- ✓ One GMB-C2165-LLVA Industrial Mother board
- ✓ One SATA III Cable
- ✓ One I/O Shield bracket
- ✓ One Installation Resources CD-Title

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

## **1.3. Product Specification**

- **Main Processor**
  - Intel® Dual Core/Quad Core i3/Xeon LGA1155 processor
- **Chipset**
  - Intel® C216 Express chipset
- **System BIOS**
  - Phoenix UEFI BIOS

- **Main Memory**
  - Four 240-pin DDR3 DIMM (ECC/non-ECC) socket support up to 32GB dual channel 1600/1333MHz memory
  - GMB-C2165-LLVA supports Non-ECC memory
- **Expansion Interface**
  - One PCIe x16 slot
  - One PCIe x16 slot (setting jump to support two PCIe x8 from CPU)
  - One PCIe x4 slot
  - Four PCI slots
- **SATA Interface**
  - Five SATA ports(Two SATA 6Gb/s, Three SATA 3Gb/s)
  - One CFEX (SATA 3Gb/s interface)
- **Serial Port**
  - Support four RS232 and two RS232/422/485
- **USB Interface**
  - Support Ten USB ports, four on rear I/O and six on board header for internal devices
- **Audio Interface**
  - Connector for Mic-In, Line-In and Line-Out
- **Real Time Clock/Calendar (RTC)**
  - Support Y2K Real Time Clock/Calendar
- **Watch Dog Timer**
  - Support WDT function through software programming for enable/disable and interval setting
  - General system reset
- **On-board Ethernet LAN**
  - Two Gigabit Ethernet (10/100/1000 Mbits/sec) LAN ports using Intel 82579LM & 82583V GbE Ethernet Controller
- **High Drive GPIO**
  - One pin-header for 8 bit GPIO(4bit in & 4bit out)
- **System Monitoring Feature**
  - Monitor system temperature and major power sources.
- **Outline Dimension (L x W)**
  - 304.8mm (12") X 243.8mm (9.6")

- **Power Requirements**

Item	Power ON	Full Loading 10Min	Full Loading 30Min
CPU +12V	1.90A	3.15A	3.32A
System +12V	0.93A	1.01A	0.96A
System +3.3V	0.63A	0.97A	0.90A
System +5V	2.12A	3.88A	3.85A
System+Device +12V	3.75A	4.77A	4.47A
System+ Device +5V	2.58A	4.65A	4.33A
USB Loading Test	4.76~5.02V / 530mA		

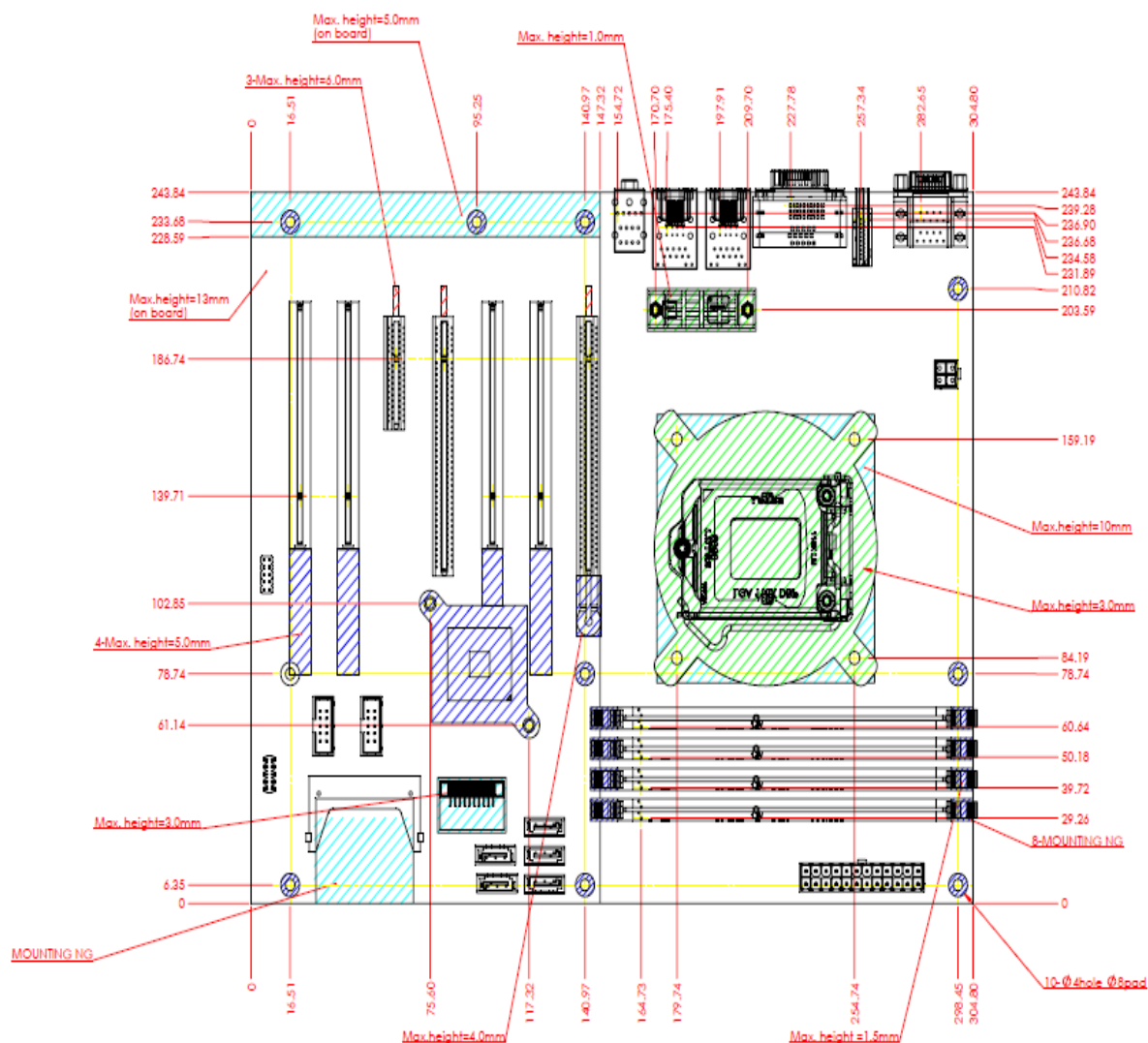
- **Configuration:**

CPU Type	Intel(R) Xeon(R) CPU E3-1275 V2 @ 3.50GHz L3 8MBytes
SBC BIOS	CONTEC, Inc. GMB-C2165-LLVA Rev.:R1.00.W1 (06102013)
Memory	WARIS DDR3 ECC-DIMM 1600/8GB (hynix H5TQ4G83MFR) x 4
VGA Card	ONBOARD Intel(R) HD Graphics P4000
VGA Driver	Intel(R) HD Graphics P4000 Version:9.17.10.2753
LAN Card	ONBOARD Intel(R)82579LM Gigabit Network Connection
LAN Driver	Intel(R)82579LM Gigabit Network Connection Version:11.14.32.0
LAN Card	ONBOARD Intel(R)82583V Gigabit Network Connection
LAN Driver	Intel(R)82583V Gigabit Network Connection Version:11.11.43.0
Audio Card	ONBOARD Intel(R) Display Audio
Audio Driver	Intel(R) Display Audio Version:6.14.0.3090
Audio Card	ONBOARD Realtek High Definition Audio
Audio Driver	Realtek High Definition Audio Version:6.0.1.6649
Chip Driver	Intel(R) Chipset Device Software Version:9.3.0.1019
USB3.0Driver	Intel(R) USB 3.0 eXtensible Host Controller Version:1.0.4.225
SCSI Card	Adaptec SCSI Card 29160LP

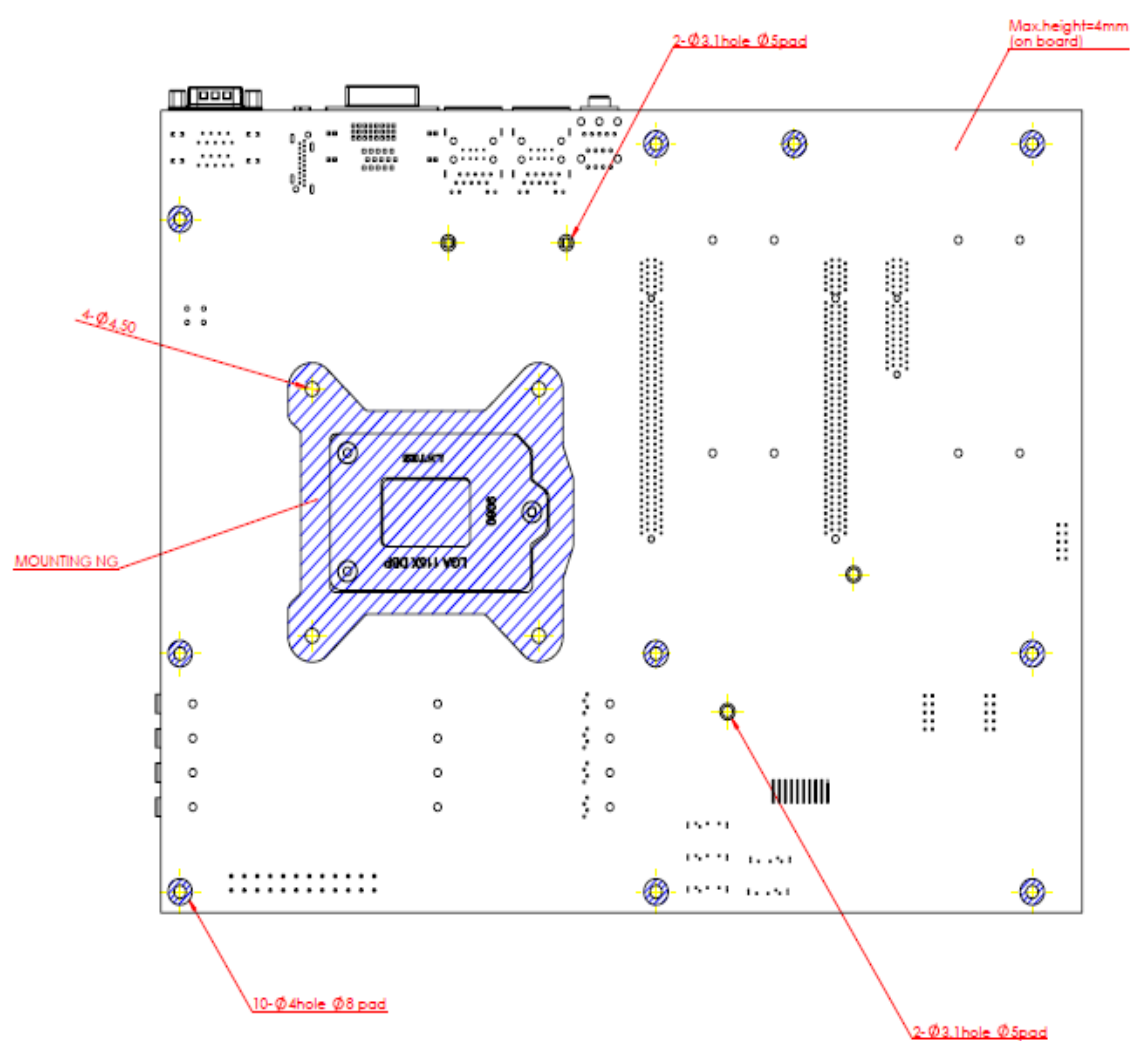
<b>SCSI HDD</b>	SEAGATE ST39173W
<b>SATA HDD</b>	Seagate ST250DM000 250GB
<b>CDROM</b>	ASUS DRW-24D3ST DVD-ROM
<b>Power Supply</b>	CONTEC ORION-D4601

- 
- **Operating Temperature**  
0 °C ~ 60 °C
- **Storage temperature**  
-20 ~ 80 °C
- **Relative Humidity**  
0% ~ 90%, non-condensing

### 1.3.1 Mechanical Drawing

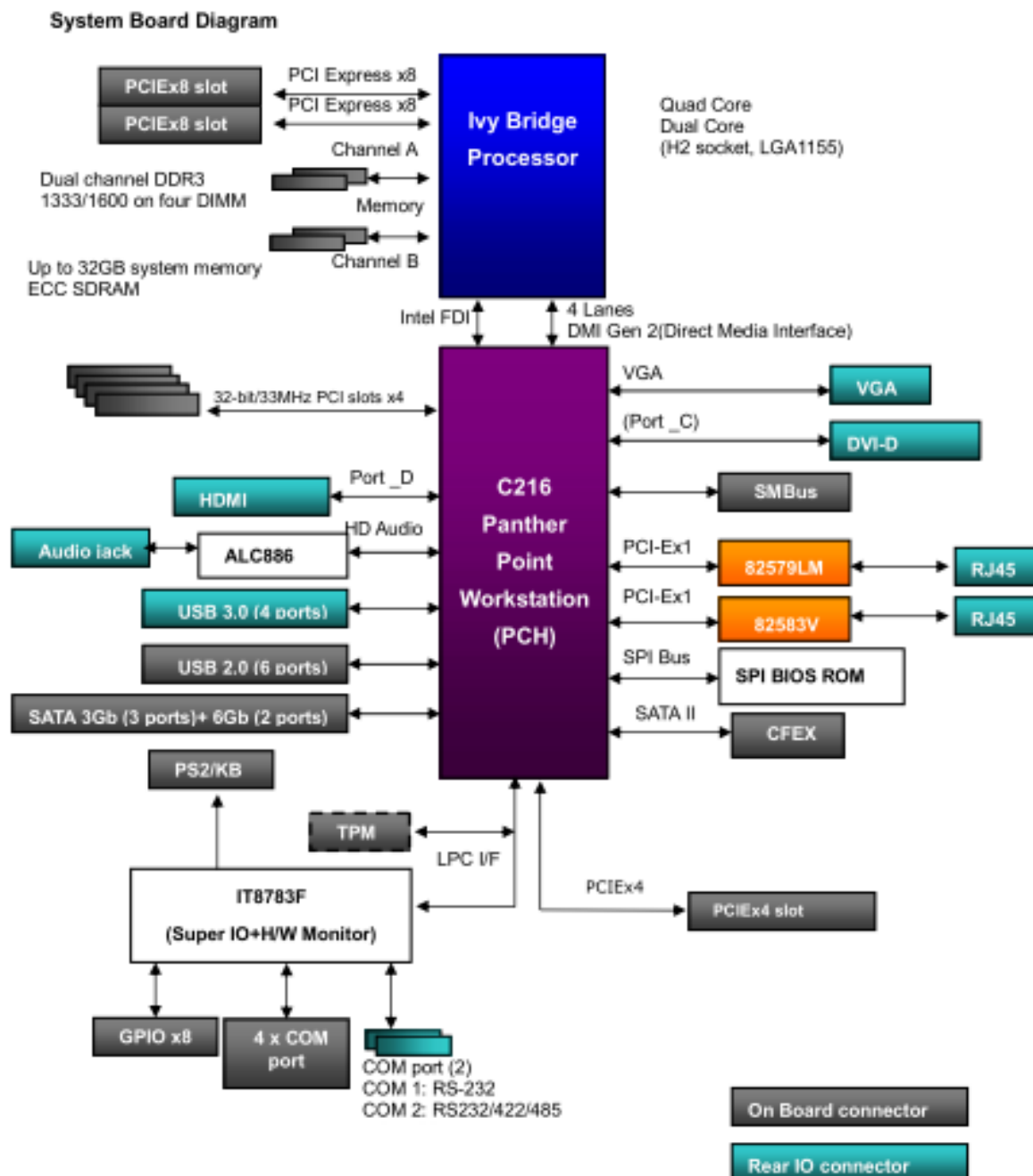






## 1.4. System Architecture

All of details operating relations are shown in GMB-C2165-LLVA System Block Diagram.



**GMB-C2165-LLVA System Block Diagram**

## 2. Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on GMB-C2165-LLVA are in the proper position. The default settings shipped from factory are marked with an asterisk (★).

### 2.1 Jumper Setting

In general, jumpers on the single board computer are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for “Not Connect”.

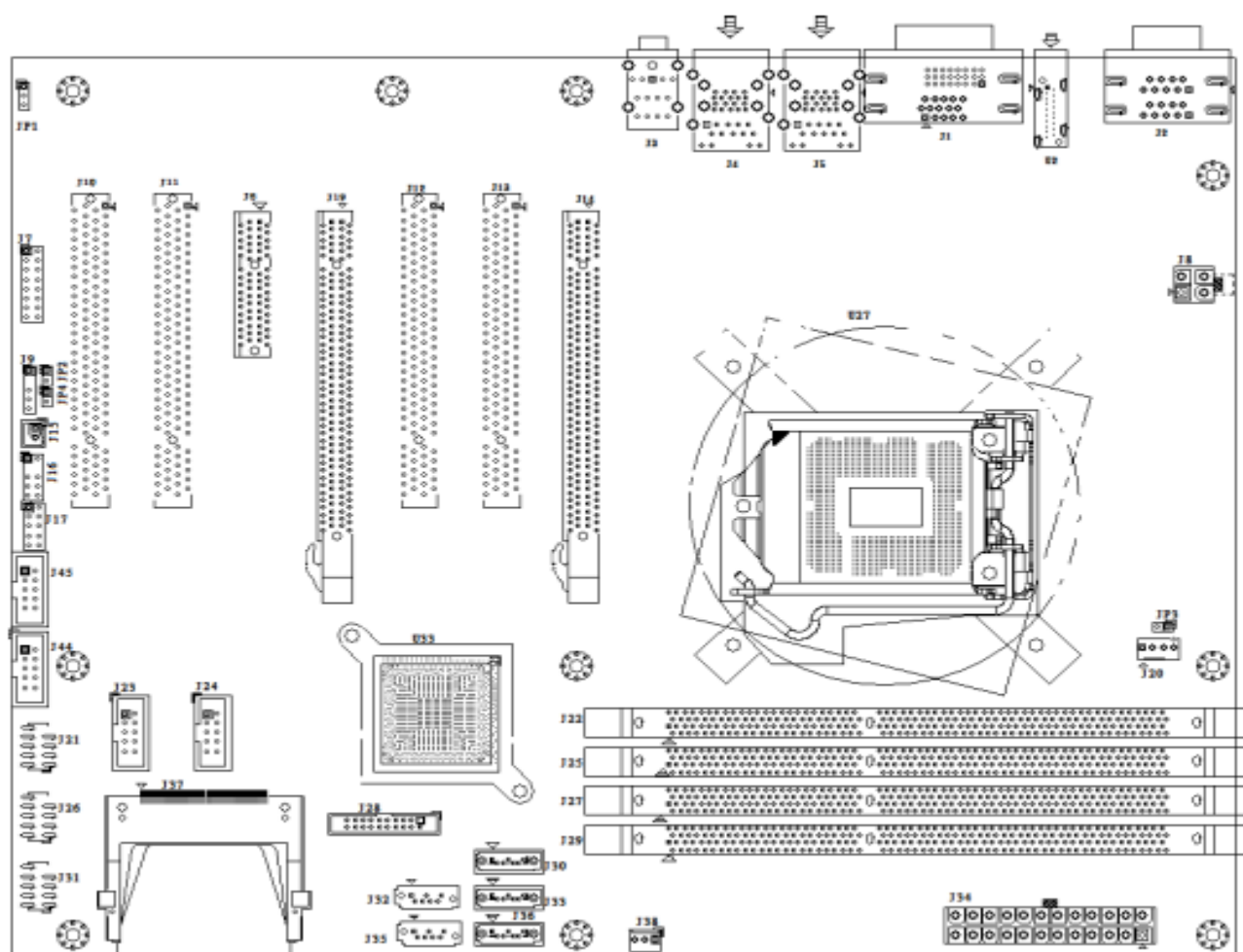


Figure 1-1 GMB-C2165-LLVA Top-side Jumper and Connector Locations

## Pin Assignments of Connectors

### JP1: Clear CMOS



PIN No.	Signal Description
1-2	Normal
2-3	Clear CMOS

### JP2: ATX / AT Mode Select



PIN No.	Signal Description
1-2 short	ATX emulation AT mode
1-2 open	ATX mode ★

### JP3: Control CFG to Select PCIE x16 or x8

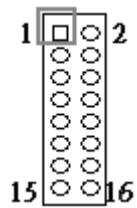


PIN No.	Signal Description
1-2 short	select x8
1-2 open	select x16

### JP4: Control Switch to Select PCIE x16 or x8



PIN No.	Signal Description
1-2 short	select x8
1-2 open	select x16

**J7: Front Panel System Connector**

PIN No.	Signal Description	PIN No.	Signal Description
1	PWR_LED(+)	2	Speaker(+)
3	PWR_LED(-)	4	N/C
5	J4 LAN1_ACT(+)	6	N/C
7	J4 LAN1_LINK(-)	8	Speaker(-)
9	J5 LAN2_LINK(-)	10	Power Button
11	J5 LAN2_ACT(+)	12	GND
13	HDD_LED(+)	14	GND
15	HDD_LED(-)	16	Rest

**J8: ATX 4Pin 12V Power Connector**

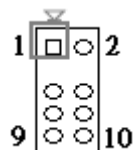
PIN No.	Signal Description
1	Ground
2	Ground
3	+12V
4	+12V

**J9: SMBus Connector**

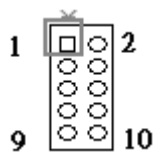
PIN No.	Signal Description
1	SMBus_CLK
2	N/C
3	Ground
4	SMBus_DAT
5	+5V

**J15: Case Open Connector**

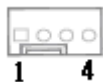
PIN No.	Signal Description
1	GND
2	Case open

**J16: External Keyboard/Mouse Connector**

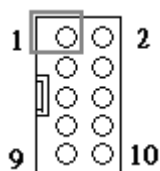
PIN No.	Signal Description	PIN No.	Signal Description
1	Mouse Data	2	Keyboard Data
3	N/C	4	N/C
5	Ground	6	Ground
7	PS2 Power	8	PS2 Power
9	Mouse Clock	10	Keyboard Clock

**J17: GPIO**

PIN No.	Signal Description	PIN No.	Signal Description
1	LPC_GP60	2	LPC_GP64
3	LPC_GP61	4	LPC_GP65
5	LPC_GP62	6	LPC_GP66
7	LPC_GP63	8	LPC_GP67
9	GND	10	Vcc

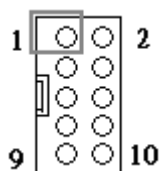
**J20: CPU FAN Power Connector**

PIN No.	Signal Description
1	Ground
2	+12V
3	Fan on/off output
4	Fan Speed control

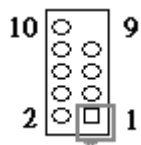
**J23/24: COM3/COM4 Serial Port Connector**

PIN No.	Signal Description	PIN No.	Signal Description
1	DCD (Data Carrier Detect)	2	DSR (Data Set Ready)
3	RXD (Receive Data)	4	RTS (Request to Send)

5	TXD (Transmit Data)	6	CTS (Clear to Send)
7	DTR (Data Terminal Ready)	8	RI (Ring Indicator)
9	GND (Ground)	10	N/C

**J44/45: COM5/COM6 Serial Port Connector**

PIN No.	Signal Description	PIN No.	Signal Description
1	DCD (Data Carrier Detect)	2	DSR (Data Set Ready)
3	RXD (Receive Data)	4	RTS (Request to Send)
5	TXD (Transmit Data)	6	CTS (Clear to Send)
7	DTR (Data Terminal Ready)	8	RI (Ring Indicator)
9	GND (Ground)	10	N/C

**J21/J26/J31: External USB Connector**

PIN No.	Signal Description	PIN No.	Signal Description
1	5V Dual	2	5V Dual
3	USB-	4	USB-
5	USB+	6	USB+
7	Ground	8	Ground
9	5V Dual	10	N/C



**J38: SYSTEM FAN Power Connector**

PIN No.	Signal Description
1	Ground
2	Fan speed control
3	Fan on/off output

**2.2 Connector Allocation**

I/O peripheral devices are connected to the interface connectors.

Connector Function List

Connector	Function	Remark
J1	DVI & VGA Port	
J2	COM PORT	COM2 Support 232/422/485
J3	Audio connector	
J4	USB 0&1/100+Giga Lan Connector (LAN1) 82579LM	
J5	USB 2&3/100+Giga Lan Connector (LAN2) 82583V	
J6	PCI-E x4 Slot	Support x4 signal
J7	Front Panel System Connector	
J8	ATX 4Pin 12V Power Connector	
J9	SMBUS HEADER	
J10、J11、J12、J13	PCI Slot	
J14	PCI-E x16 Slot	Support PCI-E Gen3
J15	Case Open Connector	
J16	External Keyboard/ Mouse Connector	

J17	8Bit GPIO Connector	
J19	PCI-E x16 Slot	Support SLI Function
J20	CPU FAN Power Connector	
J21、J26、J31	External USB Connector	
J22、J25、J27、J29	DIMM	
J23、J24、J44、J45	COM3/COM4/COM5/COM6 Serial Port Connector	
J28	TPM(Trusted Platform Module) Connector	
J30、J33、J36	SATA Connector(3Gb/s)	
J32、J35	SATA Connector(6Gb/s)	
J34	ATX Power	
J37	CFEX Slot	
J38	System FAN Power Connector	
U2	HDMI Port	
JP1	Clear CMOS	
JP2	ATX / AT Mode Select	
JP3	Control CFG to Select PCIE x16 or x8	
JP4	Control Switch to Select PCIE x16 or x8	

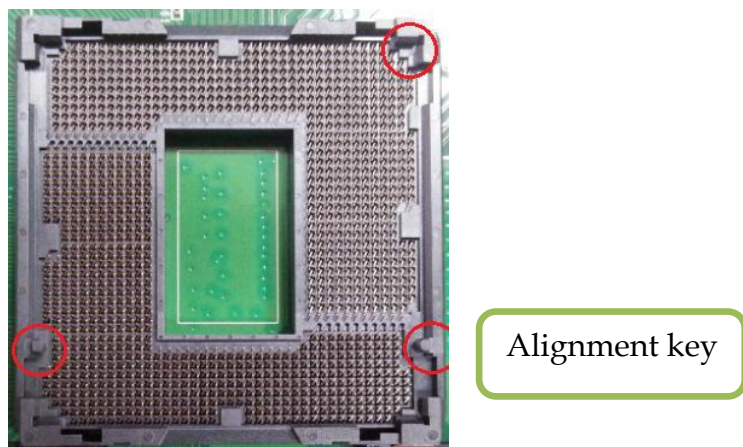
### 3. System Installation

This chapter provides the instructions to set up the system. The additional information is enclosed to help you set up onboard devices

#### 3.1 Intel® Dual Core/Quad Core processor

##### LGA-1155 CPU Socket

In the top, right corner of the CPU Socket is Pin1, and the red two circles are alignment key under the picture



##### LGA-1155 CPU

In the top, the Yellow Triangle of the CPU is Pin1.



Please remember to locate the alignment keys on the CPU socket of the motherboard and the notches on the CPU.

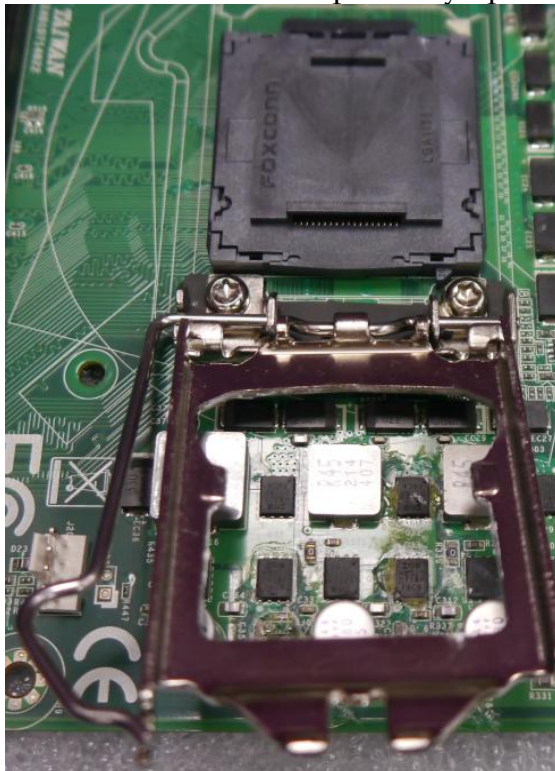
## LGA-1155 CPU Installation Steps

Before install the CPU, please make sure to turn off the power first!!

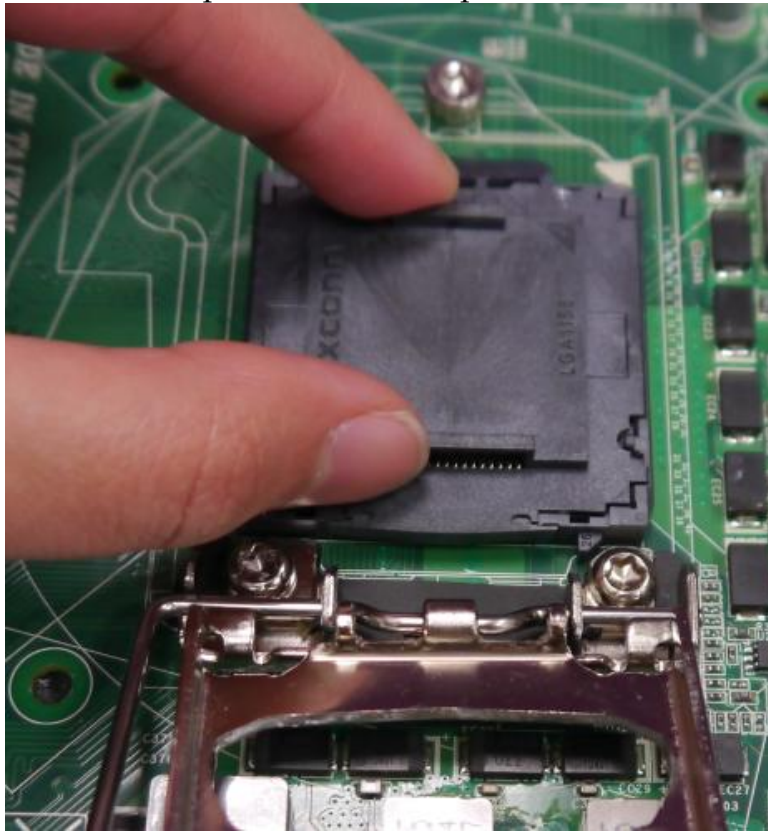
1. Open the load lever.



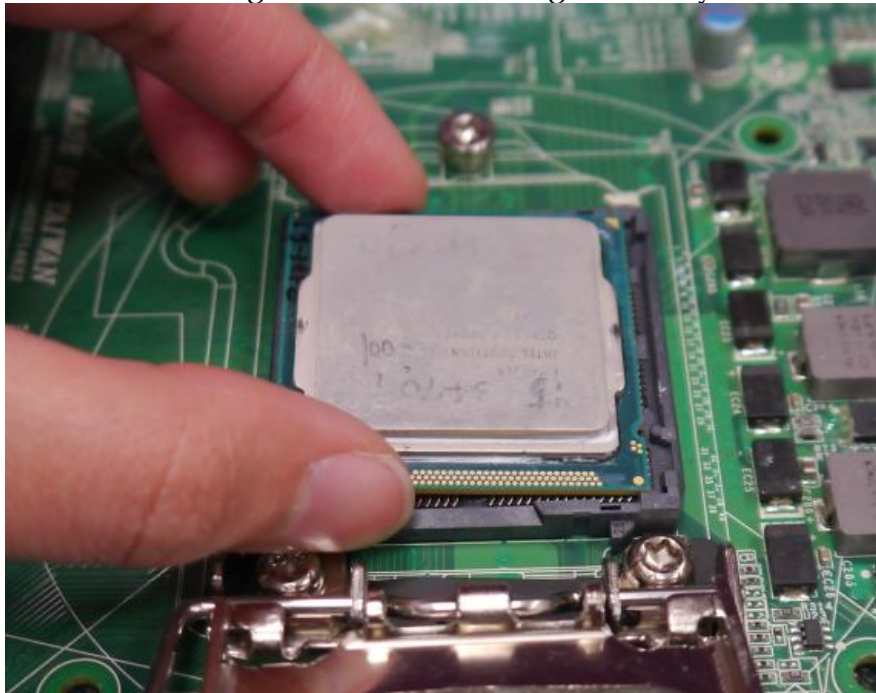
2. Lift the load lever up to fully open



3. Remove the plastic cap on the CPU socket. Before you install the CPU, always cover it to protect the socket pin.



4. After confirming the CPU direction for correct mating, put down the CPU in the socket housing frame. Note that alignment keys are matched.

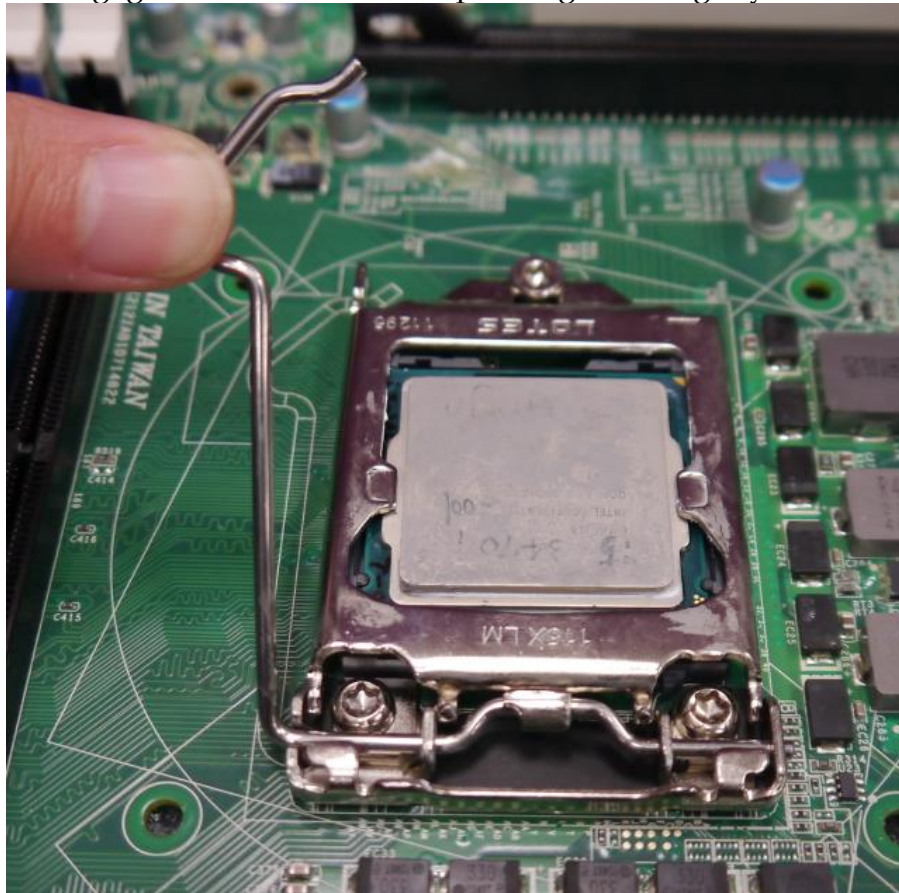




5. Make sure the CPU has been seated well into the socket. If not, take out the CPU and reinstall.



6. Engage the load lever while pressing down lightly onto the load plate.



7. Push the CPU socket lever back into its locked position.



8. Please make sure four hooks are in proper position before you install the core.

### 3.2 Main Memory

GMB-C2165-LLVA provide 4x240 pin DIMM sockets (Dual Channel) which supports Dual channel non-ECC 1333/1600 DDR3-SDRAM and 32GB DDR3 ECC memory, non-register function. The maximum memory can be up to 32GB. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be set to either one double-sided DIMM in one DIMM socket or two single-sided DIMM in both sockets.

Beware of the connection and lock integrity from memory module to socket. Inserting improperly it will affect the system reliability.

Before locking, make sure that all modules have been fully inserted into the card slots

**Note:**

To insure the system stability, please do not change any of DRAM parameters in BIOS setup to modify system the performance without acquired technical information.

### 3.3 Installing the Single Board Computer

To install your GMB-C2165-LLVA into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position.

Step 2 : Install and configure CPU and memory module at right position.

Step 3 : Place GMB-C2165-LLVA into the dedicated position in the system.

Step 4 : Attach cables to existing peripheral devices and secure it.

#### **WARNING**

Please ensure that SBC is properly inserted and fixed by mechanism.

#### **Note**

Please refer to section 3.3.1 to 3.3.5 to install INF/VGA/LAN/Audio/AMT drivers.

#### **3.3.1 Chipset Component Driver**

GMB-C2165-LLVA uses state-of-art Intel® Panther Point chipset. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for previous Windows Operating Systems such as Windows XP, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in GMB-C2165-LLVA CD-title.

Moreover, if using some old OS, the driver may not be supported anymore. We recommend changing the different OS to comply with this new chipset.

#### **3.3.2 Intel® HD Graphics Family**

With latest Intel® Quad Core and Dual core series structure (Ivy Bridge), GMB-C2165-LLVA Intel® HD Graphic 4000 is built in with CPU. Therefore 2nd Generation Core and 3rd

Generation Core CPUs provide HD integrated Graphic support sharing on board physical memories. GMB-C2165-LLVA has both internal VGA/DVI-D/HDMI interface. This combination makes GMB-C2165-LLVA an excellent piece of multimedia hardware. With no additional video adaptor, this onboard video will usually be the system display output. By adjusting the BIOS setting to disable on-board VGA, an add-on PCI-Express Graphic card can take over the system display. You can find very easily this graphic driver in GMB-C2165-LLVA CD-title.

※To use Intel® Integrated HD Graphic, it's required to choose the CPU which has Integrated Graphic built-in. Otherwise there will be no display whatsoever.



### 3.3.3 Intel® PROSet Gigabit Ethernet Controller

#### Drivers Support

Please find Intel® 82583V and 82579LM LAN driver form GMB-C2165-LLVA CD-title.

### 3.3.4 Audio Controller

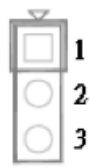
Please find Realtek ALC886-GR (Intel® High Definition Audio driver) form GMB-C2165-LLVA CD-title.

### 3.3.5 Intel® Active Management Technology (Intel® AMT)

Please find the latest Intel® AMT 8.0 driver from GMB-C2165-LLVA CD-title.

## 3.4 Clear CMOS Operation

### JP1: CLEAR CMOS



JP1	Function
1-2 Short	Normal Operation
2-3 Short	Clear CMOS Contents

## 3.5 WDT Function

The Watchdog Timer of motherboard consists of 8-bit programmable time-out counter and a control and status register.

### WDT Controller Register

There are two PNP I/O port addresses that can be used to configure WDT.

2Eh: EFIR (Extended Function Index Register, for identifying CR index number)

2Fh: EFDR (Extended Function Data Register, for accessing desired CR)

### WDT Control Mode Register

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

GMB-C2165-LLVA allows users to control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process. A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately. To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to ITE IT8783F data sheet.

There are two PNP I/O port addresses that can be used to configure WDT,

- 1) 0x2E:EFIR (Extended Function Index Register, for identifying CR index number)
- 2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)

### WDT Control Command Example

```
#include <stdio.h>
#include <conio.h>
#include <dos.h>

#define SIO_Port 0x2E
#define SIO_Port2 0x4E
#define GPIO_LDN 0x07

void Enter_IT8783_SIO() {
    outportb(SIO_Port, 0x87);
    outportb(SIO_Port, 0x01);
    outportb(SIO_Port, 0x55);
    outportb(SIO_Port, 0x55);
}
```

```

void Set_LDN(unsigned char LDN) {
    outportb(SIO_Port, 0x07);
    outportb(SIO_Port+1, LDN);
    printf("LDN=%x\n", LDN);
}

void Set_Register(unsigned char offset, unsigned char value) {
    outportb(SIO_Port, offset);
    outportb(SIO_Port+1, value);
    printf("Write offset:%x = %x\n", offset, value);
}

int main(void) {
    printf("test string\n");
    Enter_IT8783_SIO();

    Set_LDN(GPIO_LDN);

    Set_Register(0x72, 0xC0);
    Set_Register(0x73, 0x05);
    printf("System will reset in 5 seconds\n");

    return 0;
}

```

## 3.6 GPIO

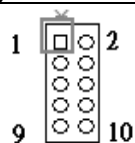
The motherboard provides 4 input/output ports that can be individually configured to perform a simple basic I/O function.

### GPIO Pin Assignment

The GMB-C2165-LLVA provides 4 input/output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

The GPIO port is located on J17 shown as follows. Please note: Do not short the Pin 9 and Pin 10 of the J17!

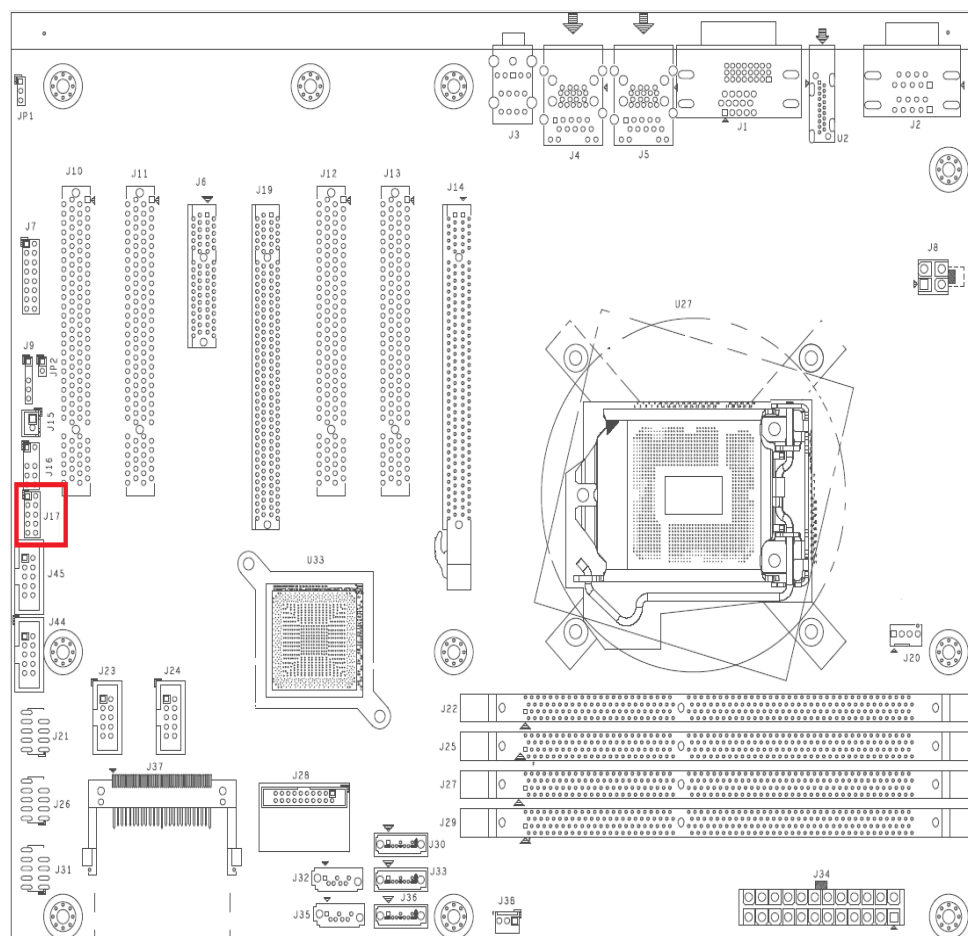
The control for the GPIO signals is handled through a separate 1-byte I/O space.

**J17: General Purpose I/O Connector**

PIN No.	Signal Description	PIN No.	Signal Description
1	LPC_GP60	2	LPC_GP64
3	LPC_GP61	4	LPC_GP65
5	LPC_GP62	6	LPC_GP66
7	LPC_GP63	8	LPC_GP67
9	GND	10	Vcc

**Note:**

All General Purpose I/O ports can only apply to standard TTL±5% signal level (0V/5V), and each Fan.



**GPIO Control Command Example (C Language)**

```

/*****
Sample Code for ITE series SIO GPIO Access
SIO IO INDEX : 0x2E
GPIO IO BASE : 0x0A00
GPIO PIN Define:
Pin 1 : GP60
Pin 2 : GP61
Pin 3 : GP62
Pin 4 : GP63
Pin 5 : GP64
Pin 6 : GP65
Pin 7 : GP66
Pin 8 : GP67
*****/

#include <stdio.h>
#include <conio.h>
#include <string.h>
#include <dos.h>

//Common defines
#define HIGH 1
#define LOW 0
#define IN 1
#define OUT 0

//Prototype defines
Int Get_IT8783_GPIOBase(
    int IOINDEX
);

void Enter_IT8783_SIO(
    int IOINDEX
);

void Exit_IT8783_SIO(
    int IOINDEX
);

void Set_IT8783_LDN(
    int IOINDEX,
    int LDN
);

```

```
int Get_IT8783_Byte_Val(
    int IOINDEX,
    int offset
);
```

```
void Set_IT8783_Byte_Val(
    int IOINDEX,
    int offset,
    int Data
);
```

```
//MAIN Code Start
int main(){
return;
}
```

```
/******
Procedure Name: Get Super IO GPIO Base address
Check defines in config file name
input 1 : INT IOINDEX
return : GPIO BASE
*****/
```

```
Int Get_IT8783_GPIOBase(int IOINDEX){
int IODATA = IOINDEX + 1;
int GPIOBASE;

//SIO Enter Key
Enter_IT8783_SIO(IOINDEX);
//Change LDN to 7 (GPIO)
Set_IT8783_LDN(IOINDEX,0x07);
//Get GPIO BASE
GPIOBASE = Get_IT8783_Byte_Val(IOINDEX,0x62) * 0x100;
GPIOBASE = GPIOBASE + Get_IT8783_Byte_Val(IOINDEX,0x63);
return GPIOBASE;
}
```

```
/******
Procedure Name : Enter IT8783 Super IO
Check defines in config file name
input 1 : INT IOINDEX
*****/

void Enter_IT8783_SIO(int IOINDEX){
int IODATA = IOINDEX + 1;
outportb(IOINDEX,0x87);
outportb(IOINDEX,0x01);
outportb(IOINDEX,0x55);
```

```
outportb(IOINDEX,0x55);
return;
}
```

/\*\*\*\*\*\*

Procedure Name: Exit IT8783 Super IO

Check defines in config file name

input 1 : INT IOINDEX

\*\*\*\*\* /

```
void Exit_IT8783_SIO(int IOINDEX) {
    int IODATA = IOINDEX + 1;
    outportb(IOINDEX,0x02);
    outportb(IODATA ,0x02);
    return;
}
```

/\*\*\*\*\*\*

Procedure Name: Change IT8783 LDN

Description: Change Super IO Logical Device Number

Input 1: INT IOINDEX

Input 2: INT LDN(Logical Device Number)

\*\*\*\*\* /

```
void Set_IT8783_LDN(
    int IOINDEX,
    int LDN ){
    int IODATA = IOINDEX+1;
    outportb(IOINDEX,0x07);
    outportb(IODATA, LDN);
    return;
}
```

/\*\*\*\*\*\*

Procedure Name: Get IT8783 offset data

Description : Get IT8783 offset byte data

Input 1: INT IOINDEX

Input 2: INT offset

return: INT Data (Byte)

\*\*\*\*\* /

```
int Get_IT8783_Byte_Val(
    int IOINDEX,
    int offset ){
    int Data;
    int IODATA = IOINDEX + 1;
    outportb(IOINDEX,offset); //set offset of data read
    Data = inportb(IODATA); //Get Data from offset
    return Data;
```

}

/\*\*\*\*\*

Procedure Name: Set IT8783 offset data

Description: Set Byte data to IT8783 offset

input 1 : INT IOINDEX

input 2 : INT offset

input 3 : INT Data

\*\*\*\*\*/

void Set\_IT8783\_Byte\_Val(

int IOINDEX,

int offset,

int Data ) {

int IODATA = IOINDEX + 1;

outportb(IOINDEX,offset);

outportb(IODATA, Data);

return;

}

/\*\*\*\*\*

Procedure Name: Set GPIO Pin 1 Mode &amp; In/Out data

Description: Set GPIO Pin I/O Mode

if GPIOMode is Input, input 2 data will

don't care and this function will return

read value.

Pin 1: GP60

input 1 : INT GPIOMode

input 2 : INT Data

Out 1: INT Data

\*\*\*\*\*/

int SET\_GPIO\_PIN1(

int GPIOMode,

int Data ) {

//GPIO Mode is Output

if(GPIOMode == 0){

Set\_IT8783\_Byte\_Val(0x2E,0xCD,Get\_IT8783\_Byte\_Val(0x2E,0xCD) |

(1&lt;&lt;0));

//if Data is HIGH

if(Data==1){

outportb(0x0A00 + 5, 1&lt;&lt;0);

}

//if Data is LOW

if(Data==0){

outportb(0x0A00 + 5, (inportb(0x0A00 + 5) &amp; ~(1&lt;&lt;0) ));

}

return NULL;



```

    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){
        Set_IT8783_Byte_Val(0x2E,0xCD,Get_IT8783_Byte_Val(0x2E,0xCD)&
~(1<<0));
        Data = inportb(0x0A00 + 5) & (1<<0);
        return Data;
    }
return NULL;
}

```

/\*\*\*\*\*

Procedure Name: Set GPIO Pin 2 Mode & In/Out data

Description: Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will  
don't care and this function will return  
read value.

Pin 2: GP61

Input 1: INT GPIOMode

Input 2: INT Data

Out 1: INT Data

\*\*\*\*\*/

```

int SET_GPIO_PIN2(
int GPIOMode,
int Data ) {
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8783_Byte_Val(0x2E,0xCD,Get_IT8783_Byte_Val(0x2E,0xCD) |
(1<<1));
        //if Data is HIGH
        if(Data==1){
            outportb(0x0A00 + 5, 1<<1 );
        }
        //if Data is LOW
        if(Data==0){
            outportb(0x0A00 + 5, (inportb(0x0A00 + 5) & ~(1<<1) ) );
        }
        return NULL;
    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){
        Set_IT8783_Byte_Val(0x2E,0xCD,Get_IT8783_Byte_Val(0x2E,0xCD) &
~(1<<1));
        Data = inportb(0x0A00 + 5) & (1<<1);
        return Data;
    }
}

```

```

    }
    return NULL;
}

```

```

/*****

```

Procedure Name: Set GPIO Pin 3 Mode & In/Out data

Description: Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will  
don't care and this function will return  
read value.

Pin 3:GP62

Input 1: INT GPIOMode

Input 2: INT Data

Out 1: INT Data

```

*****/

```

```

int SET_GPIO_PIN3(

```

```

int GPIOMode,

```

```

int Data ){

```

```

    //GPIO Mode is Output

```

```

    if(GPIOMode = 0){

```

```

        Set_IT8783_Byte_Val(0x2E,0xCD,    Get_IT8783_Byte_Val(0x2E,0xCD)    |

```

```

(1<<2));

```

```

    //if Data is HIGH

```

```

    if(Data==1){

```

```

        outportb(0x0A00 + 5, 1<<2 );

```

```

    }

```

```

    //if Data is LOW

```

```

    if(Data==0){

```

```

        outportb(0x0A00 + 5, (inportb(0x0A00 + 5) & ~(1<<2) ) );

```

```

    }

```

```

    return NULL;

```

```

    }

```

```

    //GPIO Mode is Input

```

```

    else if(GPIOMode = 1){

```

```

        Set_IT8783_Byte_Val(0x2E,0xCD,    Get_IT8783_Byte_Val(0x2E,0xCD)    &

```

```

~(1<<2));

```

```

        Data = inportb(0x0A00 + 5) & (1<<2);

```

```

        return    Data;

```

```

    }

```

```

return NULL;

```

```

}

```

```

/*****

```

Procedure Name: Set GPIO Pin 4 Mode & In/Out data

Description: Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will  
don't care and this function will return  
read value.

Pin 4: GP63

Input 1 : INT GPIOMode

Input 2: INT Data

Out 1: INT Data

```

***** /
int SET_GPIO_PIN4(
int GPIOMode,
int Data ) {
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8783_Byte_Val(0x2E,0xCD,    Get_IT8783_Byte_Val(0x2E,0xCD)    |
(1<<3));
        //if Data is HIGH
        if(Data==1){
            outportb(0x0A00 + 5, 1<<3 );
        }
        //if Data is LOW
        if(Data==0){
            outportb(0x0A00 + 5, (inportb(0x0A00 + 5) & ~(1<<3) ) );
        }
        return NULL;
    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){
        Set_IT8783_Byte_Val(0x2E,0xCD,    Get_IT8783_Byte_Val(0x2E,0xCD)    &
~(1<<3));
        Data = inportb(0x0A00 + 5) & (1<<3);
        return    Data;
    }
return NULL;
}

/*****

```

Procedure Name: Set GPIO Pin 5 Mode & In/Out data

Description: Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will  
don't care. and this function will return  
read value.

Pin 5: GP64

Input 1: INT GPIOMode

Input 2: INT Data

Out 1: INT Data

```

***** /
int SET_GPIO_PIN5(
int GPIOMode,
int Data ){
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8783_Byte_Val(0x2E,0xCD,    Get_IT8783_Byte_Val(0x2E,0xCD)    |
(1<4));
        //if Data is HIGH
        if(Data==1){
            outportb(0x0A00 + 5, 1<4 );
        }
        //if Data is LOW
        if(Data==0){
            outportb(0x0A00 + 5, (inportb(0x0A00 + 5) & ~(1<4) ) );
        }
        return NULL;
    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){
        Set_IT8783_Byte_Val(0x2E,0xCD,    Get_IT8783_Byte_Val(0x2E,0xCD)    &
~(1<4));
        Data = inportb(0x0A00 + 5) & (1<4);
        return    Data;
    }
return NULL;
}

/*****

```

Procedure Name: Set GPIO Pin 6 Mode &amp; In/Out data

Description: Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will  
don't care and this function will return  
read value.

Pin 6: GP65

Input 1: INT GPIOMode

Input 2: INT Data

Out 1: INT Data

```

***** /
int SET_GPIO_PIN6(
int GPIOMode,
int Data ) {
    //GPIO Mode is Output

```

```

        if(GPIOMode = 0){
        Set_IT8783_Byte_Val(0x2E,0xCD,   Get_IT8783_Byte_Val(0x2E,0xCD)   |
(1<<5));
        //if Data is HIGH
        if(Data==1){
        outportb(0x0A00 + 5, 1<<5 );
        }
        //if Data is LOW
        if(Data==0){
        outportb(0x0A00 + 5, (inportb(0x0A00 + 5) & ~(1<<5) ) );
        }
        return NULL;
        }
        //GPIO Mode is Input
        else if(GPIOMode = 1){
        Set_IT8783_Byte_Val(0x2E,0xCD,   Get_IT8783_Byte_Val(0x2E,0xCD)   &
~(1<<5));
        Data = inportb(0x0A00 + 5) & (1<<5);
        return    Data;
        }
return NULL;
}

```

/\*\*\*\*\*

Procedure Name: Set GPIO Pin 7 Mode & In/Out data

Description: Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will  
don't care and this function will return  
read value.

Pin 7: GP66

Input 1: INT GPIOMode

Input 2: INT Data

Out 1: INT Data

\*\*\*\*\*/

```

int SET_GPIO_PIN7(
int GPIOMode,
int Data ) {
        //GPIO Mode is Output
        if(GPIOMode = 0){
        Set_IT8783_Byte_Val(0x2E,0xCD,   Get_IT8783_Byte_Val(0x2E,0xCD)   |
(1<<6));
        //if Data is HIGH
        if(Data==1){
        outportb(0x0A00 + 5, 1<<6 );
        }
}

```

```

        //if Data is LOW
        if(Data==0){
            outportb(0x0A00 + 5, (inportb(0x0A00 + 5) & ~(1<<6) ));
        }
        return NULL;
    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){
        Set_IT8783_Byte_Val(0x2E,0xCD,  Get_IT8783_Byte_Val(0x2E,0xCD)  &
~(1<<6));
        Data = inportb(0x0A00 + 5) & (1<<6);
        return Data;
    }
    return NULL;
}

/*****

```

Procedure Name: Set GPIO Pin 8 Mode & In/Out data

Description: Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will  
don't care and this function will return  
read value.

Pin 8: GP67

Input 1: INT GPIOMode

Input 2: INT Data

Out 1: INT Data

\*\*\*\*\*/

```

int SET_GPIO_PIN8(
int GPIOMode,
int Data ) {
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8783_Byte_Val(0x2E,0xCD,  Get_IT8783_Byte_Val(0x2E,0xCD)  |
(1<<7));
        //if Data is HIGH
        if(Data==1){
            outportb(0x0A00 + 5, 1<<7 );
        }
        //if Data is LOW
        if(Data==0){
            outportb(0x0A00 + 5, (inportb(0x0A00 + 5) & ~(1<<7) ));
        }
        return NULL;
    }
    //GPIO Mode is Input

```

```
        else if(GPIOMode = 1){
            Set_IT8783_Byte_Val(0x2E,0xCD,  Get_IT8783_Byte_Val(0x2E,0xCD)  &
~(1<<7));
            Data = inportb(0x0A00 + 5) & (1<<7);
            return Data;
        }
return NULL;
}
```

## 4. BIOS Setup Information

GMB-C2165-LLVA is equipped with the Phoenix BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, GMB-C2165-LLVA communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

### 4.1 Entering Setup -- Launch System Setup

Power on the computer and the system will start POST (Power on Self Test) process. When the message below appears on the screen, press <F2> key will enter BIOS setup screen.

#### Press <F2> to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt> and <Delete> keys on keyboard simultaneously.

#### Press <F1> to Run General Help or Resume

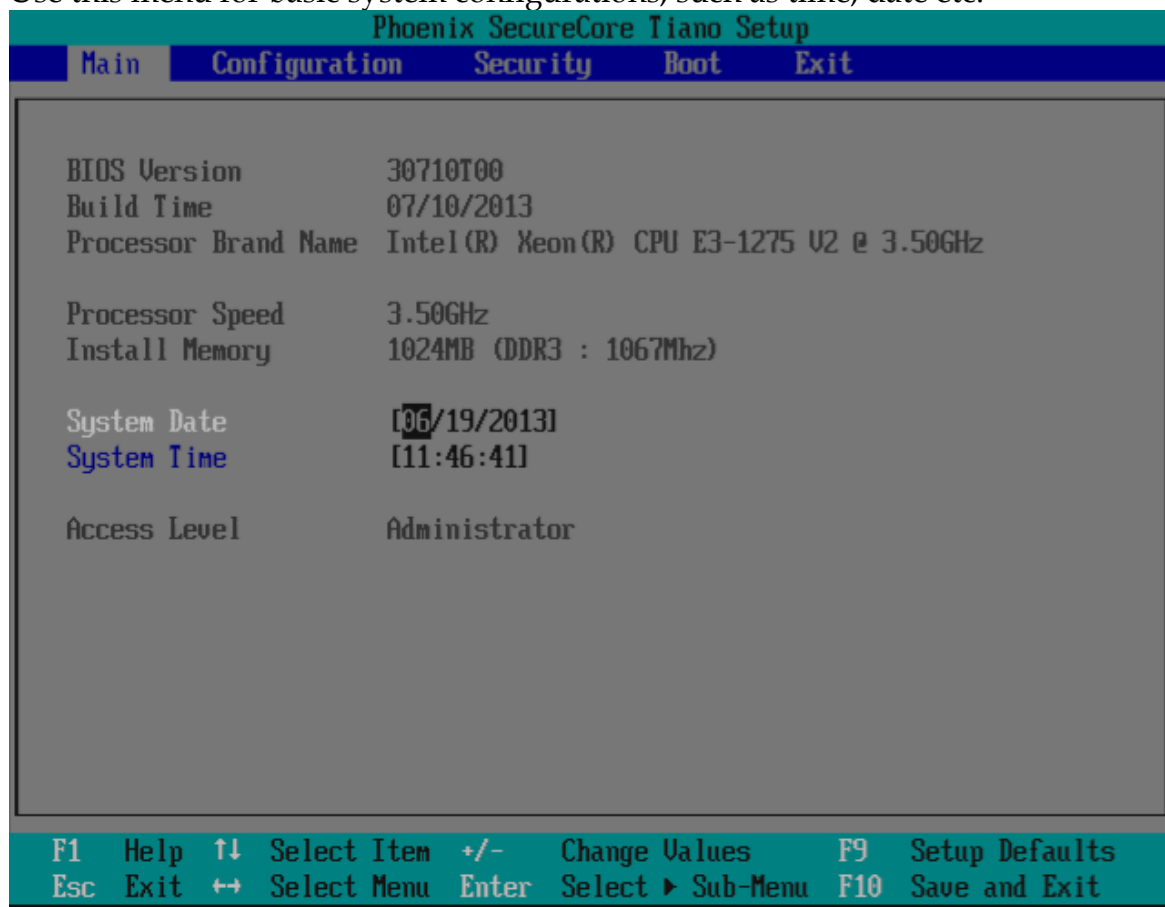
The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.





## 4.2 Main

Use this menu for basic system configurations, such as time, date etc.



### System Date

The date format is <Month>, <Day> and <Year>. Use [+] or [-] to configure system Date.

### System Time

The time format is <Hour>, <Minute> and <Second>. Use [+] or [-] to configure system Time.

4.3 Configuration

Use this menu to set up the items of special enhanced features

Phoenix SecureCore Tiano Setup									
Main		Configuration		Security		Boot		Exit	
<ul style="list-style-type: none"><li>▶ Boot Configuration</li><li>▶ PCI/PCIE Configuration</li><li>▶ Power Control Configuration</li><li>▶ CPU Configuration</li><li>▶ LAN Configuration</li><li>▶ Chipset Configuration</li><li>▶ Graphic Configuration</li><li>▶ SATA Configuration</li><li>▶ USB Configuration</li><li>▶ ME Configuration</li><li>▶ Super IO Configuration</li><li>▶ Hardware Monitor</li><li>▶ Serial Port Console Configuration</li></ul>								Item Specific Help	
								Set Boot Configuration.	
F1	Help	↑↓	Select Item	+/-	Change Values	F9	Setup Defaults		
Esc	Exit	↔	Select Menu	Enter	Select ▶ Sub-Menu	F10	Save and Exit		

Boot Configuration

Set boot configuration.

Phoenix SecureCore Tiano Setup									
		Configuration							
Boot Configuration						Item Specific Help			
<div>NumLock: <span>[ON]</span></div> <div>Quick Boot <span>[Disabled]</span></div> <div>Diagnostic Splash Screen <span>[Disabled]</span></div> <div>Diagnostic Summary Screen <span>[Disabled]</span></div> <div>Allow Hotkey in S4 resume <span>[Disabled]</span></div> <div>UEFI Boot <span>[Disabled]</span></div>						Selects Power-on state for NumLock.			
F1	Help	↑↓	Select Item	+/-	Change Values	F9	Setup Defaults		
Esc	Exit	↔	Select Menu	Enter	Select ▶ Sub-Menu	F10	Save and Exit		

**NumLock:**

Selects Power-on state for NumLock.

Choices: OFF, ON.

**Quick Boot**

Enable/Disable quick boot.

Choices: Disabled, Enabled.

**Diagnostic Splash Screen**

If you select 'Enabled' the diagnostic splash screen always displays during boot. If you select 'Disabled' the diagnostic splash screen does not displays unless you press HOTKEY during boot.

Choices: Disabled, Enabled.

**Diagnostic Summary Screen**

Display the Diagnostic summary screen during boot.

Choices: Disabled, Enabled.

**Allow Hotkey in S4 resume**

Enable hotkey detection when system resuming from Hibernate state.

Choices: Disabled, Enabled.

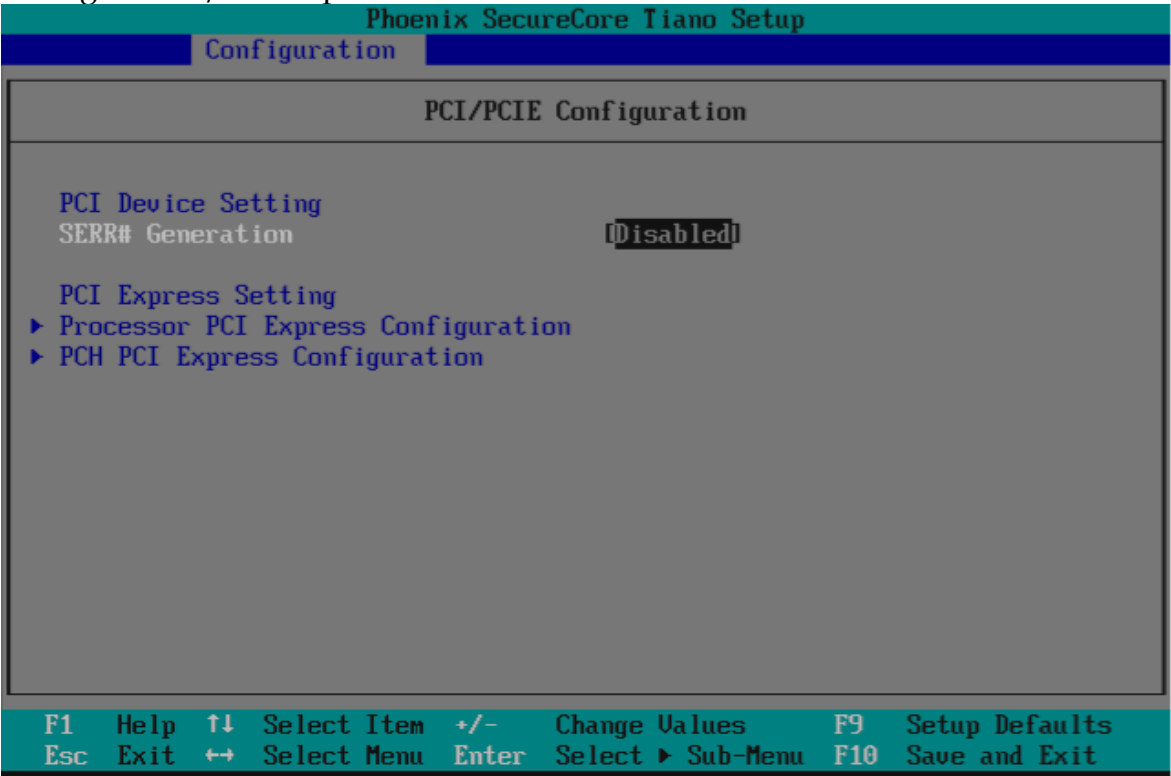
**UEFI Boot**

Enable the UEFI boot.

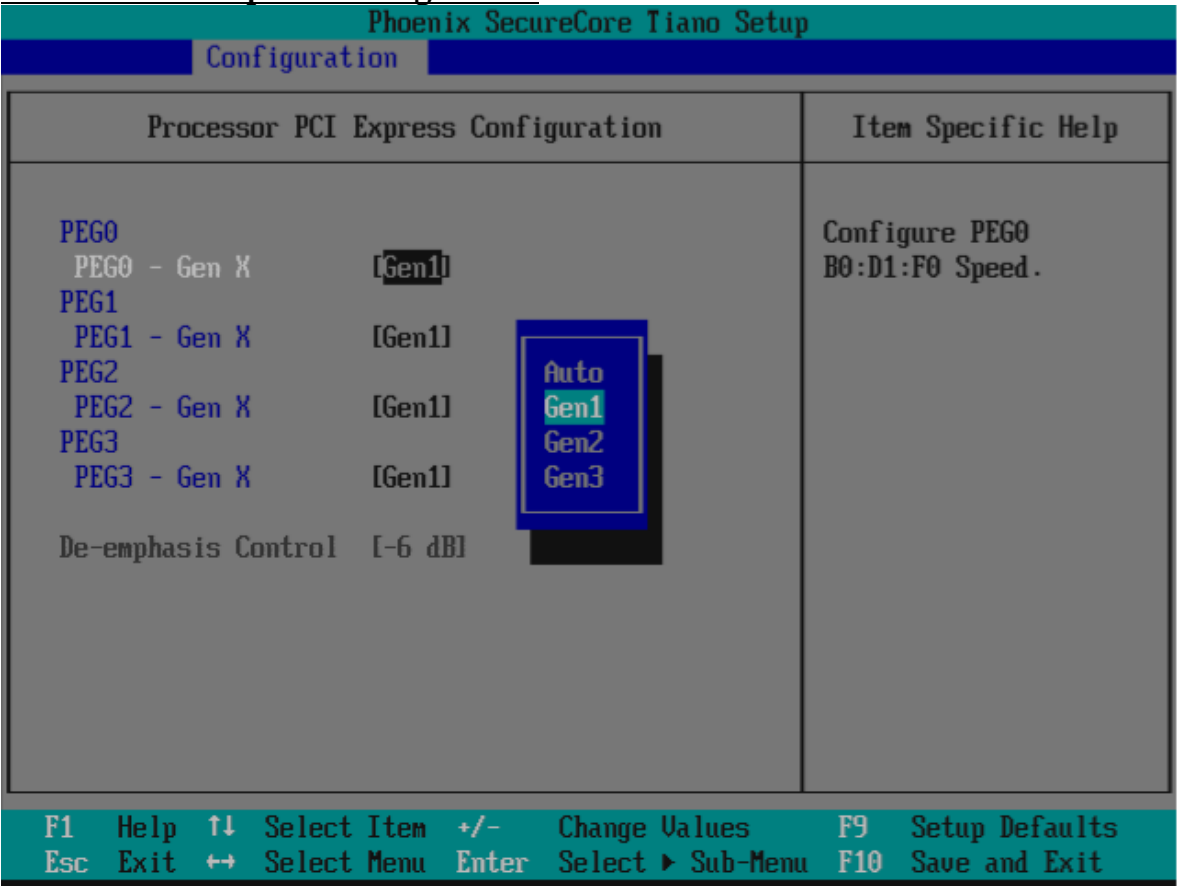
Choices: Disabled, Enabled.

PCI/PCIE Configuration

Configure PCI/PCI Express slot.



Processor PCI Express Configuration



**FEG0 PEG0 - Gen X**

Configure PFG0 B0:D0:F0 Speed.

Choices: Auto, Gen1, Gen2, Gen3

**FEG1 PEG1 - Gen X**

Configure PFG1 B0:D0:F1 Speed.

Choices: Auto, Gen1, Gen2, Gen3

**FEG2 PEG2 - Gen X**

Configure PFG2 B0:D0:F2 Speed.

Choices: Auto, Gen1, Gen2, Gen3

**FEG3 PEG3 - Gen X**

Configure PFG3 B0:D0:F3 Speed.

Choices: Auto, Gen1, Gen2, Gen3

**ICH PCI Express Configuration**

Phoenix SecureCore Tiano Setup	
Configuration	
PCH PCI Express Configuration	Item Specific Help
DMI Link ASPM Control <b>Auto</b> ▶ PCI Express Root Port 1 PCIE Port 5 is assigned to 82583V LAN PCIE Port 6 is assigned to 82579LM GbE LAN ▶ PCI Express Root Port 7 ▶ PCI Express Root Port 8	The control of active state Power Management on both NB side of the DMI Link.
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults Esc Exit ↔ Select Menu Enter Select ▶ Sub-Menu F10 Save and Exit	

**DMI Link ASPM Control**

The control of active state Power Management on both NB side of the DMI Link.

Choices: Disabled, L0s, L1, L0sL1 and Auto.

**PCI Express Root Port 1, 7, 8**

Control PCI Express root port.

Phoenix SecureCore Tiano Setup		
Configuration		
PCI Express Root Port 1		Item Specific Help
PCI Express Root Port 1	[Enabled]	Control PCI Express root port.
PCIe Speed	[Auto]	
ASPM	[Disabled]	
HOT PLUG	[Disabled]	
URR	[Disabled]	
FER	[Disabled]	
NFER	[Disabled]	
CER	[Disabled]	
SEFE	[Disabled]	
SENFE	[Disabled]	
SECE	[Disabled]	
PME Interrupt	[Disabled]	
PME SCI	[Enabled]	
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults Esc Exit ↔ Select Menu Enter Select ► Sub-Menu F10 Save and Exit		

**PCI Express Root Port 1, 7, 8**

Control PCI Express root port.

Choices: Disabled, Enabled.

**PCIe Speed**

Select PCIe Speed to Gen1 or Gen2.

Choices: Auto, Gen1, Gen2.

**ASPM**

Control PCIe Active State Power Management settings.

Choices: Disabled, L0S, L1, L0S and L1, Auto.

**HOT PLUG**

PCI Express Hot Plug Enabled/Disabled.

Choices: Disabled, Enabled.

**URR**

PCI Express Unsupported Request Reporting Enable/Disable.

Choices: Disabled, Enabled.

**FER**

PCI Express Device Fatal Error Reporting Enable/Disable.

Choices: Disabled, Enabled.

**NFER**

PCI Express Device Non-Fatal Error Reporting Enable/Disable.

Choices: Disabled, Enabled.

**CER**

PCI Express Device Correctable Error Reporting Enable/Disable.

Choices: Disabled, Enabled.

**SEFE**

Root PCI Express System Error on Fatal Error Enable/Disable.

Choices: Disabled, Enabled.

**SENFE**

Root PCI Express System Error on Non-Fatal Error Enable/Disable.

Choices: Disabled, Enabled.

**SECE**

Root PCI Express System Error on Correctable Error Enable/Disable.

Choices: Disabled, Enabled.

**PME Interrupt**

Root PCI Express PME Interrupt Enable/Disable.

Choices: Disabled, Enabled.

**PME SCI**

PCI Express PME SCI

Choices: Disabled, Enabled.

**Power Control Configuration**

Configure ACPI and RTC wake up setting.

Phoenix SecureCore Tiano Setup		
Configuration		
Power Control Configuration		Item Specific Help
ACPI Sleep State	[S3]	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Restore AC power loss	[Power Off]	
SLP_S4 Assertion stretch Enable	[Disabled]	
Wake system with Fixed Time	[Disabled]	
Wake up By PS/2 Keyboard	[Disabled]	
Wake up By PS/2 Mouse	[Disabled]	
Wake up By PCI	[Disabled]	
Wake up By PCIe	[Disabled]	
Wake up By Ring	[Disabled]	
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults Esc Exit ↔ Select Menu Enter Select ► Sub-Menu F10 Save and Exit		

**ACPI Sleep State**

Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.

Choices: S1, S3.

**Restore AC Power Loss**

Select AC Power state when power is re-applied after a power failure.

Choices: Power Off, Power On, Last State.

**SLP\_S4 Assertion stretch Enable**

Choices: Disabled, Enabled

**Wake system with Fixed Time**

Enable or disable system wake on alarm event. When Enabled, system will wake on the hr: min: sec specified.

Choices: Disabled, Enabled

**Wake up By PS/2 Keyboard**

Choices: Enabled, Disabled.



### Wake up By PS/2 Mouse

Choices: Enabled, Disabled.

### Wake up By PCI

Choices: Enabled, Disabled.

### Wake up By PCIe

Choices: Enabled, Disabled.

### Wake up By Ring

Choices: Enabled, Disabled.

### CPU configuration

Configure the specific active core(s) and advanced processor management technologies.

Phoenix SecureCore Tiano Setup		
Configuration		
CPU Configuration		Item Specific Help
Max Processor Speed	3.50 GHz	Enabled for windows XP and Linux (OS optimized for Hyper-threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading). When Disabled only one.
Processor Cores	[4]	
Intel HT technology	Not Supported	
Hyper-threading	[Enabled]	
Active Processor Cores	[All]	
Limit CPUID Maximum	[Disabled]	
Execute Disable Bit	[Enabled]	
EIST	[Disabled]	
C-States	[Disabled]	
VT-x	[Enabled]	
Local x2APIC	[Disabled]	
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults		
Esc Exit ↔ Select Menu Enter Select ► Sub-Menu F10 Save and Exit		

### Hyper-Threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When disabled only one.

Choices: Disabled, Enabled.

### **Active Processor Cores**

Select the number of physical cores to enable in each processor package.

Choices: All, 1, 2, 3.

### **Limit CUID Maximum**

Disabled for Windows XP.

Choices: Disabled, Enabled.

### **Execute Disabled Bit**

Enabled Execute Disabled functionality. Also known as Data Execution Prevention (DEP).

Choices: Disabled, Enabled.

### **EIST**

Selects Disabled or Enabled for Enhanced Intel SpeedStep Technology.

Choices: Disabled, Enabled.

### **C-States**

Selects Disabled or Enabled for CPU operating states.

Choices: Disabled, Enabled.

### **VT-x**

When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology.

Choices: Disabled, Enabled.

### **Local x2APIC**

Selects Disabled or Enabled for Advanced Programmable Interrupt Controller.

Choices: Disabled, Enabled.

**LAN Configuration**

Configure onboard LAN device.

Phoenix SecureCore Tiano Setup			
Configuration			
LAN Configuration			Item Specific Help
Intel 82579LM GbE LAN	[Enabled]		Enabled/Disabled Intel 82579LM GbE LAN.
Wake on LAN	[Enabled]		
LAN Boot ROM	[Disabled]		
Intel 82583V LAN	[Enabled]		
Wake on LAN	[Enabled]		
F1 Help ↑↓ Select Item +/- Change Values      F9 Setup Defaults Esc Exit ↔ Select Menu Enter Select ► Sub-Menu      F10 Save and Exit			

**Intel 82579LM GbE LAN**

Enabled/Disabled Intel 82579LM GbE LAN.

Choices: Disabled, Enabled.

**Wake on LAN**

Enabled/Disabled Wake on LAN Function.

Choices: Disabled, Enabled.

**LAN Boot ROM**

Control LAN Boot ROM (PXE) function.

Choices: Disabled, Enabled.

**Intel 82583V LAN**

Enabled/Disabled 82583V LAN.

Choices: Disabled, Enabled.

**Wake on LAN**

Enabled/Disabled Wake on LAN Function.

Choices: Disabled, Enabled.

**Chipset Configuration**

Configure Chipset provide feature.

Phoenix SecureCore Tiano Setup	
Configuration	
Chipset Configuration	Item Specific Help
<div>VT-d [Disabled]</div> <div>▶ NB PCIe Configuration</div> <div>▶ Memory Configuration</div> <div>▶ SB Azalia Config</div>	<div>Check to enable VT-d function on MCH.</div>
<div>F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults</div> <div>Esc Exit ↔ Select Menu Enter Select ▶ Sub-Menu F10 Save and Exit</div>	

**VT-d**

Check to enable VT-d function on MCH.

Choices: Disabled, Enabled.

**NB PCIe Configuration**

Config NB PCI Express Settings.

Phoenix SecureCore Tiano Setup					
Configuration					
NB PCIe Configuration				Item Specific Help	
Always Enable PEG [Disabled]				To Enable the PEG Slot.	
PEG ASPM [Disabled]					
F1	Help	↑↓	Select Item	+/-	Change Values
Esc	Exit	↔	Select Menu	Enter	Select ► Sub-Menu
F9	Setup Defaults				F10 Save and Exit

**Always Enable PEG**

To Enable the PEG Slot.

Choices: Disabled, Enabled.

**PEG ASPM**

Control ASPM (Active State Power Management) Support for the PEG Device. This has mp effect if PEF is not the current active service.

Choices: Disabled, Auto, ASPM L0s, ASPM L1, ASPM L0sL1.

Choices: Enabled, Disabled.

**Memory Configuration**

Memory Configuration Parameters.

Phoenix SecureCore Tiano Setup		
Configuration		
Memory Configuration		Item Specific Help
Memory Frequency	1067 MHz	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.
DIMM#0		
DIMM#1	1024 MB (DDR3)	
DIMM#2		
DIMM#3		
Max TOLUD	[2 GB]	
Memory Frequency	[Auto]	
Memory ECC Support	[Disabled]	
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults Esc Exit ↔ Select Menu Enter Select ► Sub-Menu F10 Save and Exit		

**Max TOLUD**

Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

Choices: Dynamic, 1GB, 1.25GB, 1.5GB, 1.75GB, 2GB, 2.25GB, 2.5GB, 2.75GB, 3GB, 3.25GB, 3.5GB.

**Memory Frequency**

Maximum Memory Frequency Selections in Mhz.

Choices: Auto, 1067, 1333, 1600, 1867, 2133.

**Memory ECC Support**

Selects ECC memory function Disable/Enable.

Choices: Disable, Enable.

**SB Azalia Configuration**

SB Azalia Config Parameters.

Phoenix SecureCore Tiano Setup		
Configuration		
SB Azalia Configuration		Item Specific Help
Azalia	[Enabled]	Control Detection of the Azalia device.
Azalia PME Enabled	[Disabled]	
Azalia Vci Enabled	[Disabled]	
Azalia internal HDMI codec	[Enabled]	
HDMI codec Port B	[Disabled]	
HDMI codec Port C	[Disabled]	
HDMI codec Port D	[Enabled]	
F1 Help ↑↓ Select Item +/- Change Values    F9 Setup Defaults Esc Exit ↔ Select Menu Enter Select ► Sub-Menu    F10 Save and Exit		

**Azalia**

Control detection of the Azalia device.

Choices: Disable, Enable.

**Azalia PME Enable**

Choices: Disable, Enable.

**Azalia Vci Enable**

Choices: Disable, Enable.

**Azalia Internal HDMI codec**

Choices: Disable, Enable.

**HDMI codec Port B**

Choices: Disable, Enable.

**HDMI codec Port C**

Choices: Disable, Enable.

### HDMI codec Port D

Choices: Disable, Enable.

### Graphic Configuration

Configure integrated Graphic like Boot display, video memory and external Graphic feature.

Phoenix SecureCore Tiano Setup			
Configuration			
Graphic Configuration			Item Specific Help
Primary Display	[Auto]		Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.
Internal Graphics	[Auto]		
Aperture Size	[256MB]		
DUMT Pre-Allocated	[64M]		
DUMT Total Gfx Mem	[256MB]		
Primary Boot display	[VBIOS Default]		
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults Esc Exit ↔ Select Menu Enter Select ► Sub-Menu F10 Save and Exit			

### Primary Display

Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for Switchable Gfx.

Choices: Auto, IGFX, PEG and PCI.

### Internal Graphics

Keep IGD Enabled Based on the setup options,

Choices: Auto, Disabled, Enabled.

### Aperture Size

Select the Aperture Size

Choices: 128MB, 256MB, 512MB.



**DVMT Pre-Allocated**

Select DVMT 5.0 Pre-Allocated Graphics Memory size used by the Internal Graphics Device.

Choices: 0M, 32M, 64M, 96M, 128M, 160M, 192M, 224M, 256M, 288M, 320M , 352M, 384M, 416M, 448M, 480M, 512M.

**DVMT Total Gfx Mem**

Select DVMT 5.0 Total Graphics Memory size used by the Internal Graphics Device.

Choices: 128MB, 256MB, MAX.

**Primay Boot display**

Choices: VBIOS Default, CRT, LFP, LFP2, EFP, EFP2, EFP3.

**SATA Configuration**

Configure SATA controller and view detected HDD Information.

Phoenix SecureCore Tiano Setup			
Configuration			
SATA Configuration			Item Specific Help
SATA Controller(s)	[Enabled]	▲ ▼	Enable/Disable SATA Device.
Launch Storage OpROM	[Disabled]		
SATA Mode	[AHCI]		
Serial ATA Port 0	[Empty]		
Port 0	[Enabled]		
Hot Plug	[Enabled]		
External Port	[Disabled]		
SATA Device Type	[Hard Disk Driver]		
Serial ATA Port 1	[Empty]		
Port 1	[Enabled]		
Hot Plug	[Enabled]	▼	
External Port	[Disabled]		
SATA Device Type	[Hard Disk Driver]		
Serial ATA Port 2	[Empty]		
F1 Help	↑↓ Select Item	+/- Change Values	F9 Setup Defaults
Esc Exit	↔ Select Menu	Enter Select ► Sub-Menu	F10 Save and Exit

### **SATA Controller (s)**

Determines how SATA controllers (s) operate.

Choices: Disabled, Enabled.

### **Launch Storage OpROM**

Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

Choices: Enabled, Disabled.

### **SATA Mode**

Determines how SATA controllers (s) operate.

Choices: Disabled, IDE, AHCI, and RAID.

### **Serial ATA Port 0**

Display the identity of the device attached.

Choices: Empty.

### **Port 0-4**

Enabled or Disabled SATA Port 0.

Choices: Disabled, Enabled.

### **Hot Plug**

Designates this port as Hot Pluggable.

Choices: Disabled, Enabled.

### **External Port**

External SATA Support.

Choices: Disabled, Enabled.

### **SATA Device Type**

Select "Solid State Drive" only if a Solid State Drive is connected to this SATA port.

Choices: Hard Disk Driver, Solid State Drive.

### **CFex**

Choices: Empty.

### **CFex**

Enabled or Disabled CFex Port.

Choices: Disabled, Enabled.

### **Hot Plug**

Designates this port as Hot Pluggable.

Choices: Disabled, Enabled.

### **External Port**

External SATA Support.

Choices: Disabled, Enabled.

**USB Configuration**

Configure USB controller and other advanced setting.

Phoenix SecureCore Tiano Setup		
Configuration		
USB Configuration		Item Specific Help
Legacy USB Support      [Enabled] ▶ PCH USB Configuration		Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
F1	Help    ↑↓    Select Item    +/-    Change Values	F9    Setup Defaults
Esc	Exit    ↔    Select Menu    Enter    Select ▶ Sub-Menu	F10    Save and Exit

**Legacy USB Support**

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

Choices: Enabled, Disabled.

**PCH USB Configuration**

Control each of the USB ports disabling.

Phoenix SecureCore Tiano Setup	
Configuration	
PCH USB Configuration	Item Specific Help
USB Ports Per-Port Disable Disabled	Control each of the USB ports disabling.
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults Esc Exit ↔ Select Menu Enter Select ► Sub-Menu F10 Save and Exit	

**USB Ports Per-Port Disable**

Control each of the USB ports disabling.

Choices: Enabled, Disabled.

**ME Configuration**

Configure Management Engine Technology Parameters.

Phoenix SecureCore Tiano Setup							
Configuration							
ME Configuration			Item Specific Help				
ME FW Version	8.1.0.1265		Enable/Disable Intel(R) Management Engine.				
ME Firmware	Intel(R) ME SMB firmware						
Intel(R) ME	<u>Enabled</u>						
F1	Help	↑↓	Select Item	+/-	Change Values	F9	Setup Defaults
Esc	Exit	↔	Select Menu	Enter	Select ► Sub-Menu	F10	Save and Exit

**Intel (R) ME**

Enable/Disable Intel (R) Management Engine.

Choices: Enabled, Disabled.

## Super IO Configuration

Configure LPC Super IO.

Configure L1 Supervisor:

Phoenix SecureCore Tiano Setup			
Configuration			
SIO Configuration		Item Specific Help	
Serial Port			
Serial Port 1	[3F8 / IRQ4]		
Serial Port 2	[2F8 / IRQ3]		
Serial Port 3	[3E8 / IRQ5]		
Serial Port 4	[2E8 / IRQ6]		
Serial Port 5	[220 / IRQ7]		
Serial Port 6	[228 / IRQ11]		
COM2 Configuration		[RS-232]	
Watch Dog Timer			
Watch Dog Timer Select	[Disabled]		
Case Open			
Case Open Warning	[Disabled]		
F1	Help	↑↓	Select Item
Esc	Exit	↔	Select Menu
+/-	Change Values		
Enter	Select	▶	Sub-Menu
F9	Setup Defaults		
F10	Save and Exit		

### Serial Port 1-6

Choices: Disabled, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ5, 2E8/IRQ6, 220/IRQ7, 228/IRQ11.

### COM2 Configuration

Select Com2 Configuration.

Choices: RS-232, RS-422, RS-485.

### Watch Dog Timer Select

Choices: Disabled, 30 secs, 1 min, 2 mins and 3 mins.

### Case Open Warning

Choices: Disabled, Enable.

**Hardware Monitor**

Provide on board sensor reading information. (Show only)

Phoenix SecureCore Tiano Setup

Configuration

Hardware Monitor

▶ CPU Fan Feature

CPU Temperature	[ 50 °C ]
System Temperature	[ 30 °C ]
CPU Fan	[ 5973 RPM]
System Fan	[ N/A ]
VCORE	[ 0.97 V ]
1.5V	[ 1.48 V ]
VCC3	[ 3.39 V ]
VCC	[ 5.13 V ]
+12V	[ 12.22 V ]
-12V	[ -11.74 V ]
5VSB	[ 5.02 V ]

F1	Help	↑↓	Select Item	+/-	Change Values	F9	Setup Defaults
Esc	Exit	↔	Select Menu	Enter	Select ▶ Sub-Menu	F10	Save and Exit

**CPU Fan Feature**

Phoenix SecureCore Tiano Setup

Configuration

Smart Fan Control Feature

CPU Fan Control

Smart Fan Control [Disabled]

F1	Help	↑↓	Select Item	+/-	Change Values	F9	Setup Defaults
Esc	Exit	↔	Select Menu	Enter	Select ▶ Sub-Menu	F10	Save and Exit

**Smart Fan Control**

Choices: Enabled, Disabled.

**Serial Port Console Configuration**

Configure console redirection on serial port.

Phoenix SecureCore Tiano Setup	
Configuration	
Serial Port Console Configuration	Item Specific Help
Serial Port 1 Console Redirection [Disabled]	Control Console Redirection enable/disable.
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults Esc Exit ↔ Select Menu Enter Select ► Sub-Menu F10 Save and Exit	

**Console Redirection**

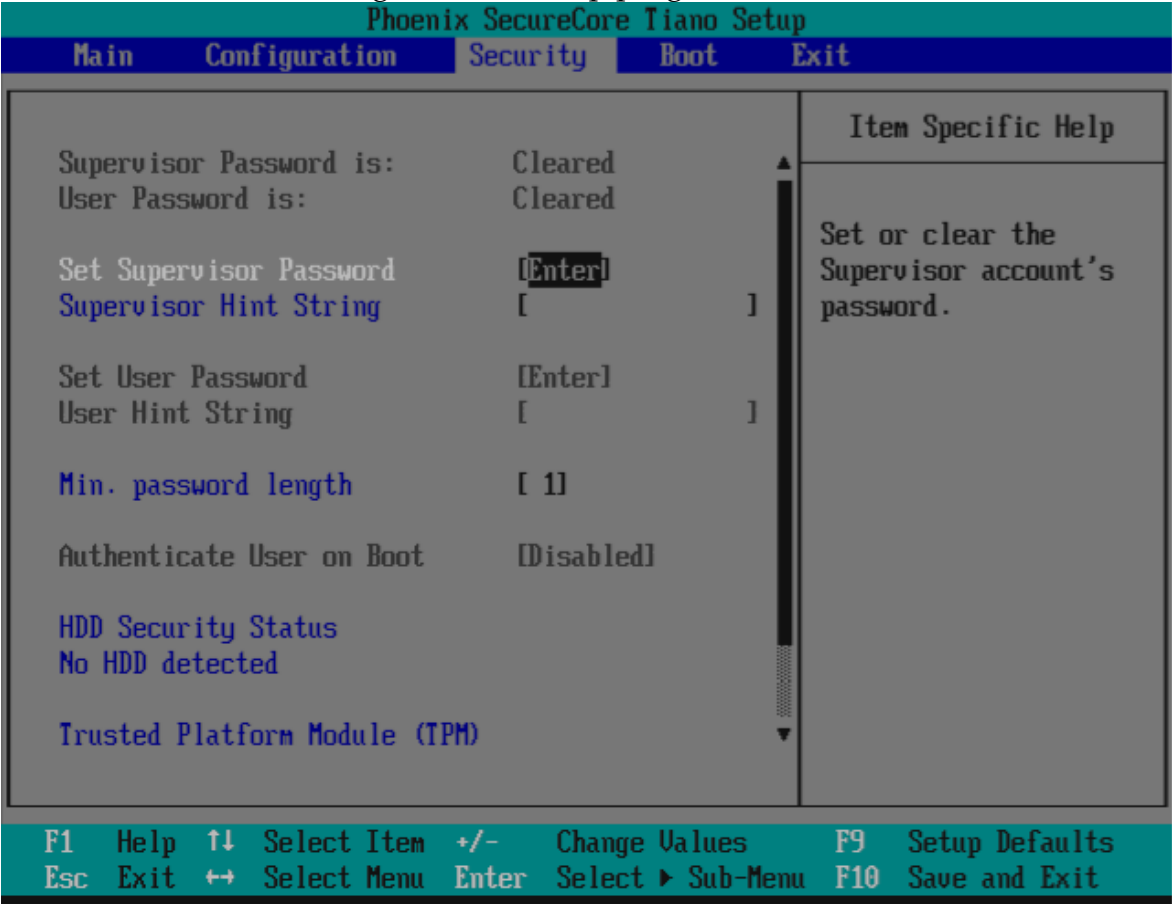
Control Console Redirection enable/disable.

Choices: Enabled, Disabled.



4.4 Security

This section lets you set security passwords to control access to the system at boot time and/or when entering the BIOS setup program.



**Set Supervisor Password**

Set or clear the Supervisor account's password.

**Supervisor Hint String**

Press Enter to type Supervisor Hint String.

**Set User Password**

Set or clear the User account' password.

**Supervisor Hint String**

Press Enter to type User Hint String.

**Min. password length**

Set the minimum number of characters for password (1-20).

4.5 Boot

Use this menu to specify the priority of boot devices.

Phoenix SecureCore Tiano Setup

Main

Configuration

Security

Boot

Exit

Boot Priority Order

1. ATA HDD0:

2. USB HDD:

3. USB CD:

4. USB FDD:

5. ATAPI CD:

6. ATA HDD1:

7. ATA HDD2:

8. ATA HDD3:

9. ATA HDD4:

10. CFex:

11. Other HDD:

12. BEV:

13. PCI LAN:

Item Specific Help

Keys used to view or configure devices: ↑ and ↓ arrows Select a device. '+' and '-' move the device up or down. 'Shift + 1' enables or disables a device. 'Del' deletes an unprotected device.

F1 Help ↑↓ Select Item +/- Change Values

F9 Setup Defaults

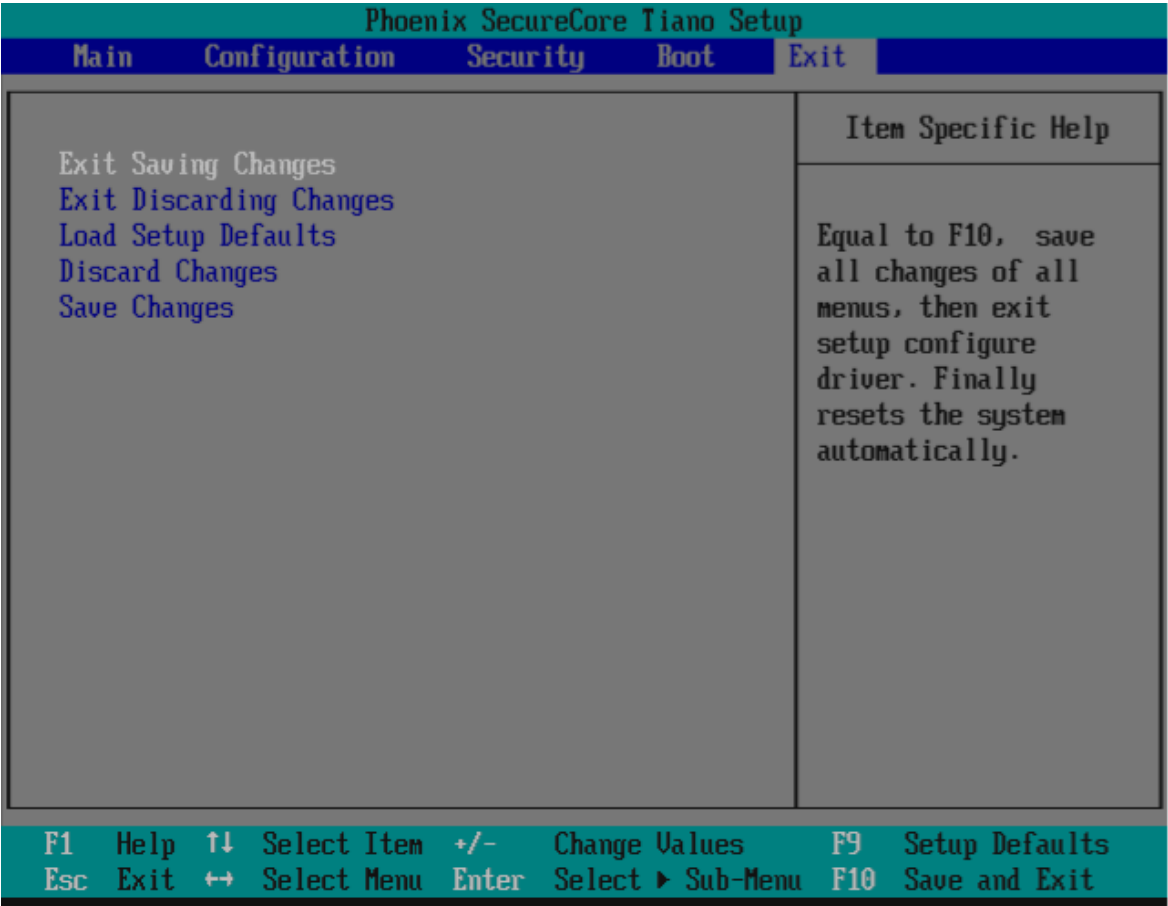
Esc Exit ↔ Select Menu Enter Select ▶ Sub-Menu

F10 Save and Exit

Boot Priority Order

Keys used to view or configure devices:↑and↓arrows Select a device. '+' and '-'move the device up or down. 'Shift + 1' enabled or disables a device. 'Del' deletes an unprotected device.

4.6 Exit



**Exit Saving Changes**  
Equal to F10, save all changes of all menus, then exit setup configure driver. Finally resets the system automatically.

**Exit Discarding Changes**  
Equal to ESC, never save changes, then exit setup configure driver.

**Load Setup Defaults**  
Equal to F9. Load standard default values.

**Discard Changes**  
Load the original value of this boot time. Not the default Setup value.

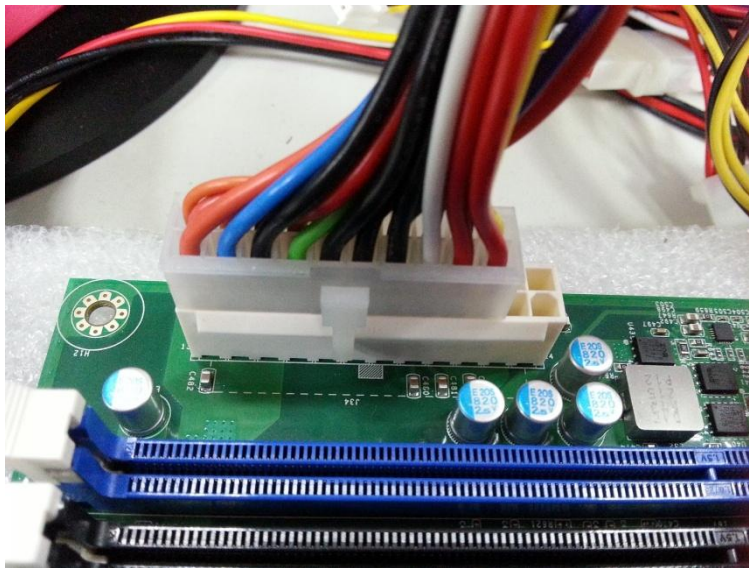
**Save Changes**  
Save all changes of all menus, but do not reset sys

## 5. Troubleshooting

This chapter provides a few useful tips to quickly get GMB-C2165-LLVA running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

### 5.1 Hardware Quick Installation

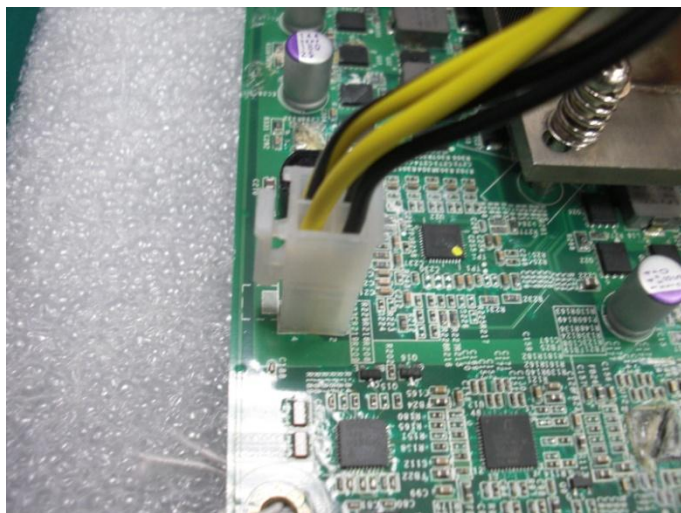
#### ATX Power Setting



GMB-C2165-LLVA supports ATX. Therefore, there is no other setting that really needs to be set up. However, there are only two connectors that must be connected – J8 (4 pins CPU +12V main power connector) & J34 (24 pins ATX Power Connector)

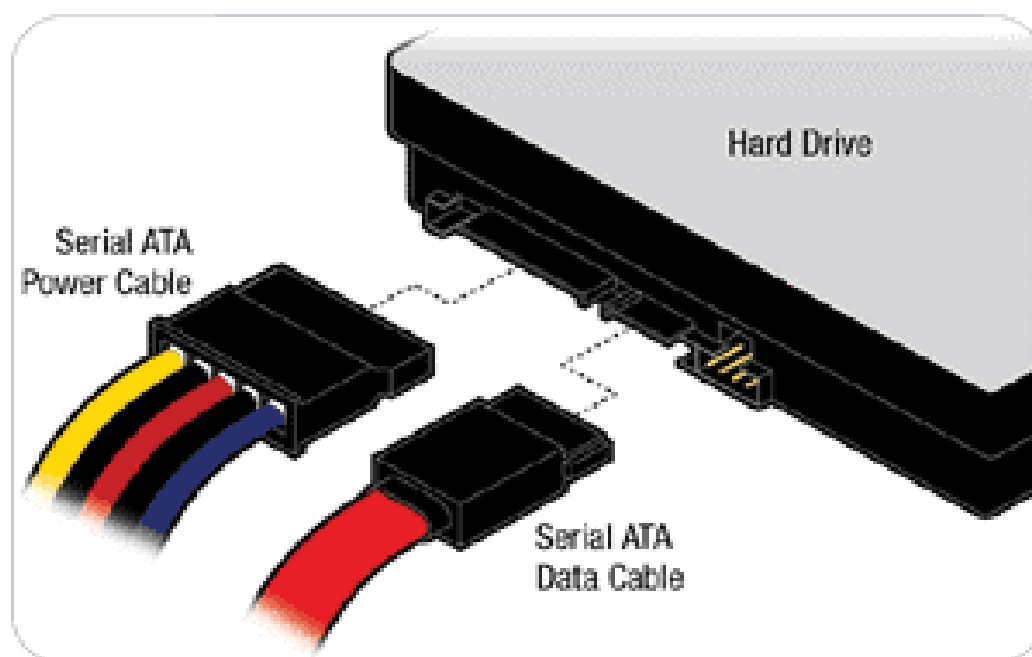
#### **ATX Power Connector**

#### **4-Pins CPU Main Power Connector**



### Serial ATA Hard Disk Setting for IDE/RAID/AHCI mode

Unlike IDE bus, each Serial ATA channel can only connect to one SATA hard disk at a time; there are total five connectors, SATA1~5 port. The installation of Serial ATA is simpler and easier than IDE, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation. All you need to operate IDE, RAID (0/1/5/10) and AHCI application for system, please follow up setting guide in BIOS setup utility



## 5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power. CPU, CPU Fan, 204-pin DDR3 memory, keyboard, mouse, floppy drive, SATA hard disk, DVI connector, but it only can use on DVI-D function, doesn't support DVI-I function, device power cables, ATX accessories are good examples that deserve attention. With no assurance of

properly and correctly accommodating these modules and devices, it is very possible

to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with GMB-C2165-LLVA , it is recommended, when going with the boot-up sequence, to hit “DEL” key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

### Loading the default optimal setting

When prompted with the main setup menu, please scroll down to “Load Optimal Defaults”, press “Enter” and “Y” to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that CONTEC has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

### Improper disable operation

There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the COM1/COM2 ports, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

Disable COM1 serial port to release IRQ #4

Disable COM2 serial port to release IRQ #3

Etc...

A quick review of the basic IRQ mapping is given below for your reference.

Interrupt Request Lines IRQ		
IRQ#	Current Use	Default Use
IRQ 0	Unused	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	【Unassigned】	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	【Unassigned】	Usable IRQ

IRQ 6	System ROM	Diskette Event
IRQ 7	Unused	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	【Unassigned】	Usable IRQ
IRQ 10	【Unassigned】	Usable IRQ
IRQ 11	【Unassigned】	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	【Unassigned】	Usable IRQ

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

### 5.3 System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used for your reference.

System Memory Address Map		
Memory Area	Size	Description
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0070-0548	19K	DOS
0549-0FC2	41K	Program Area
0FC3-9B7F	558K	【Available】
9B80-9D7F	8K	Unused
First Meg -- Conventional memory end at 630K --		
9D80-9DFF	2K	Extended BIOS Area

9E00-9FFF	8K	Unused
A000-AFFF	64K	VGA Graphics
B000-BFFF	32K	Unused
C000-CE5F	32K	VGA Text
CE60-EFFF	57K	Video ROM
	134K	Unused